V7/ Issue 2 /2012

NANOCHIP FAB SOLUTIONS

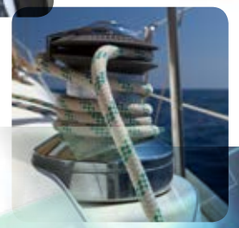
Solutions for Factory and Equipment Efficiency

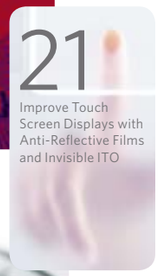
Navigating through a changing industry

APPLIED MATERIALS®

NANOCHIP FAB SOLUTIONS

CONTENTS





PLUS:

NANOCHIP
FAB SOLUTIONS

PUBLISHER
Dana Tribula
dana_tribula@amat.com

EDITOR-IN-CHIEF
Liz Baird
liz_baird@amat.com

PRODUCTION MANAGER
Gary Dagastine

CONTRIBUTING WRITERS
Gary Dagastine
gdagastine@nycap.rr.com

Katherine Derbyshire
kderbyshire@thinfilmmfg.com

David Lammers
dlammers@austin.rr.com

NANOCHIP is published by
Applied Materials, Inc.

www.appliedmaterials.com

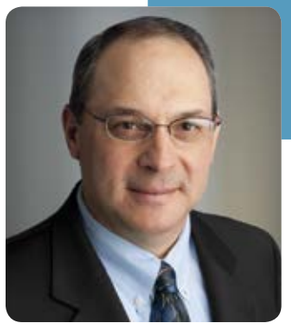
To receive extra copies of NANOCHIP or to add colleagues to the mailing list, please email your
• Name
• Title
• Company
• Business address
to *nanochip_editor@amat.com*

NANOCHIP is now available in an environmentally friendly online version. Please send an email to *nanochip_editor@amat.com* to request online delivery.

APPLIED MATERIALS®

INTERESTING TIMES:
THE EVOLUTION OF NEW AND OLD IN THE SEMICONDUCTOR INDUSTRY

A Letter from Charlie Pappis



CHARLIE PAPPIS
GROUP VICE PRESIDENT AND GENERAL MANAGER, APPLIED GLOBAL SERVICES

Right now, the technology challenges our industry faces seem more complex than ever. In addition to traditional scaling, we are seeing rapid changes in materials and device structures to sustain the pace of productivity increases the industry has generated over the last several decades. On top of that, the industry is working on the next transition in wafer size: 450mm. Wafer size transitions are nothing new; 100mm was "state of the art" when I first joined Applied Materials over two decades ago. However, these intricacies and ever increasing demands on defect densities make this a particularly interesting time for our industry.

We're seeing major changes in both semiconductor technologies and industry players, and a number of those are explored in this issue of *Nanochip Fab Solutions.* For example, the success of EUV lithography has become so critical to the industry that ASML has now forged agreements with some of their key customers—Intel, Samsung, TSMC—to invest in their business. That change may accelerate both 450mm and EUV adoption, but significant risks need to be mitigated in both.

And then there are the challenges of ramping volume production for atomic level device designs, with technologies such as 3D architectures, through-silicon vias (TSVs), and FinFETs. The costs and risks associated with these rapid changes are causing some major chip makers to rethink their strategies and vie for niche positions. In some cases we see companies going fabless or exiting the chip-making business altogether.

Times are interesting too for the solar and display markets. Although solar cell manufacturing capacity still exceeds demand, we see very strong growth in the end markets. In the display market, manufacturers are no longer focused solely on large scale LCD screens for televisions. The explosion in "everything touch"— from tablets and smartphones, to all sorts of electronic appliances and gadgets, has fueled a resurgence of factories producing the smaller displays on an earlier generation of equipment.

The evolution of the 200mm business is also an interesting story. In this issue of *Nanochip Fab Solutions*, we look at how Spansion is achieving higher productivity and lower costs in its 200mm fab, and examine emerging applications for power devices, TSV structures and MEMS devices that are breathing new life into 200mm fabs. You'll also learn what Applied Materials is doing to ensure that parts remain available for these older tools. Other articles focus on some of the manufacturing challenges around process control, and how to manage particles and film uniformities in a high volume production environment.

So these are interesting times indeed—and I hope, interesting reading for our *Nanochip Fab Solutions* subscribers.

THICK FILMS, NEW PROCESSES, DIFFERENT MATERIALS— WHAT'S NEXT FOR 200MM PRODUCTION

BY MIKE ROSA

Electric vehicles, remotely powered sensor networks, inventive handheld devices and other new products depend on enabling technologies now in various stages of development. These include advanced power ICs, 3D chip modules, thin-film batteries and novel MEMS devices—all of which are currently manufactured on 200mm wafers.

Although this may change as device footprint, form factor and average selling price (ASP) become greater factors, scaling and migration to larger wafer sizes are not currently priorities for these applications. What is in short supply is continued innovation in the areas of new materials development, thick film processing, and thin/thick wafer handling.

Producing and integrating these diverse devices and circuits require a variety of semiconductor fabrication techniques ranging from complex dry etch processes to the deposition of different types of thick and thin films. Examples include aluminum nitride (AlN), germanium (Ge), thick oxides (≥40µm thick), thick epitaxial films (>150µm) and thick aluminum (Al) (≥10µm), magnetically aligned films such as nickel iron (NiFe), and low-temperature CMOS-compatible films, including silicon germanium (SiGe).

Understandably, producing this variety of devices for myriad applications isn't easy, and the task is made even harder by today's economic imperatives. Technology development must be volume-production worthy and cost-effective to generate the highest possible financial returns, both for customers and toolmakers. This class of emerging technologies is among the most price sensitive, with ASPs far lower than one dollar, so the bulk of the global production takes place on ≤ 200mm-compatible toolsets.

Over the longer term, however, as devices continue to be refined and evolve in their design and process complexity, there will be staged migration to 300mm tools for extremely high volume production. Early examples of technology segments that may benefit from this transition include power devices and MEMS.

Here is a look at a few technologies needed to produce the devices and circuits for some of tomorrow's most exciting products.

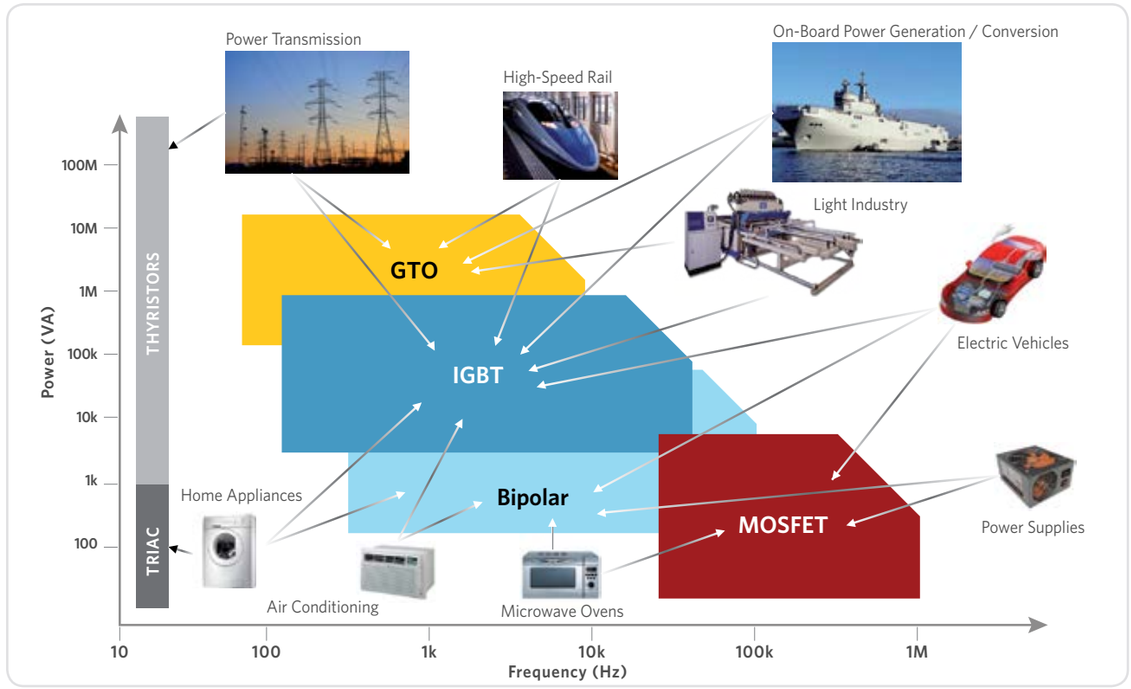


Figure 1. New power semiconductors are needed for power conversion, regulation and control in a broad range of applications. (Courtesy of Yole Développement.)

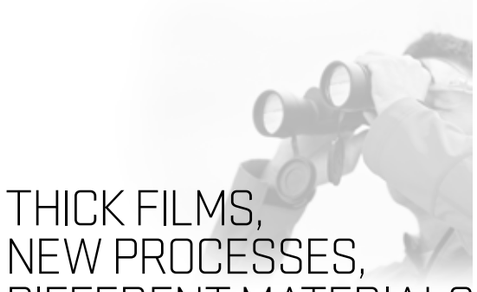
POWER ELECTRONICS

Semiconductor technology development historically has been aimed at producing ICs with greater functionality and speed. But with globally heightened interest in environmentally sensitive alternative energy solutions for a number of applications (see figure 1) comes a greater focus on the issue of power management. Today that means not only power conversion and voltage/current regulation and control, but also the ability to do these things at higher speeds and at increasing levels of power.

In the renewable energy area, for example, key goals are to increase the efficiency and power output of wind turbine generators. Next-generation power conversion systems are being developed that can more efficiently and reliably step down the output power to desired voltages, rectify it and go on to perform other power conversion functions.

Hybrid/electric vehicles are another huge opportunity. They have sophisticated electrical systems that use many power ICs for power conversion and enable electronic systems to act as substitutes for power-hungry, heavier, and less-efficient electromechanical and hydraulic components.

Advanced power semiconductors will depend on four key technologies: thick Al for heat transfer, thick epi, deep reactive ion etch (DRIE) for trench formation, and the ability to handle thin wafers and the stresses relevant to their extremely thin material layers.



THICK FILMS, NEW PROCESSES, DIFFERENT MATERIALS—

WHAT'S NEXT FOR 200MM PRODUCTION

These four technologies are needed for each of the main types of advanced power semiconductors:

- **Discrete power transistors:** Super junction transistors (SJTs) switch quickly and can handle high currents, voltages and power levels. Today there are two ways to fabricate the SJT device (see figure 2). The first is a thick epi deposition doped in one area. The deposition is repeated several times to build thickness and then it is annealed (see figure 3). With the second method, a trench is etched and then filled with doped epi material.
- **Insulated gate bipolar transistors (IGBTs):** Used where both high efficiency and fast switching are required, IGBTs combine the characteristics of both MOSFETs and bipolar transistors. They are often found in power conversion/conditioning applications.
- **Bipolar-CMOS-DMOS (BCD) circuits:** So-called "smart power" technology that combines high-density logic circuitry with fully dielectrically isolated power switches and analog components for complex power management functions.

3D ICs: TSVs AND THIN WAFERS

To address the cost and technical challenges associated with continued device scaling, one emerging alternative is to stack chips and wafers in a 3D configuration to achieve higher circuit density and a smaller overall footprint, and to integrate chips made with different technologies. Key to the 3D architecture is the ability to fabricate through-silicon vias (TSVs). These high aspect ratio vias run vertically through the stack and are filled with metal to interconnect the various chips.

Manufacturers had expected to use 200mm tools for TSV development and 300mm tools for volume production. However, other emerging technologies are being developed on 200mm wafers and some of them require stacking and isolation, which can leverage TSV processes. Therefore, manufacturers decided to also develop TSV technologies on 200mm tools.

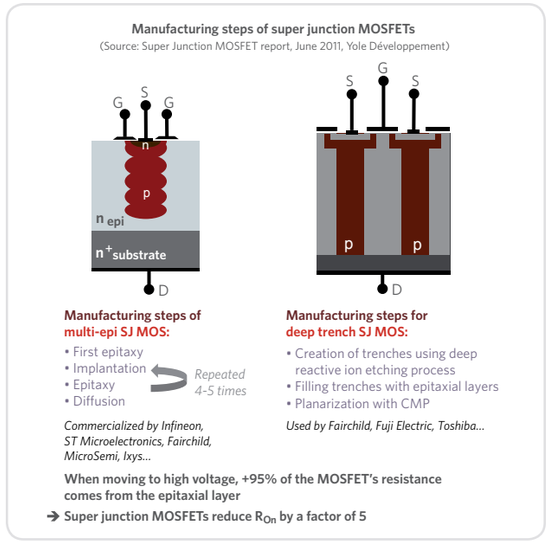


Figure. 2. The two main methods used to produce the thick films required by super junction MOSFETs. (Courtesy of Yole Développement.)

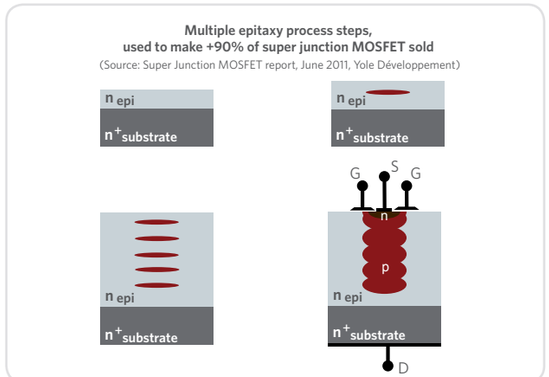


Figure 3. The lengthy and repetitive thick epi deposition process—while widely used—is less efficient and precise than the alternative dry etching and filling approach now in production. (Courtesy of Yole Développement.)

2011 TOP 10 PROVIDERS OF POWER DEVICES
1. Infineon
2. Mitsubishi Electric
3. Toshiba
4. STMicroelectronics
5. International Rectifier
6. Fuji Electric
7. Fairchild
8. Vishay
9. Renesas
10. Semikron

Table 1. A globally diverse group of IC manufacturers is currently engaged in power electronics R&D on 200mm tools.[1]

APPLICATION	PROCESS PARAMETERS
Etch (Si etch)	• High etch rate and uniformity • Small scallop size • High resist selectivity • Low cost of owership (CoO)
CVD (liner and passivation)	• Excellent thickness uniformity and coverage • Thermal budget • Adhesion to PVD Ta/TiN barriers
PVD (barrier/seed)	• Continuous barrier coverage • Cu seed coverage on via even on scalloped sidewall
ECD (electro chemical deposition)	• Enhanced bottom-up fill, wide process window, reduced over-burden • Lower thickness requirements for ionized Cu seed • Lower combined CoO PVD B/S+ECD+CMP
CMP (polishing)	• High removal rate • Excellent thickness uniformity • Low cost of consumables (CoC)

Figure 4. Process capabilities and associated parameters required for TSV production.

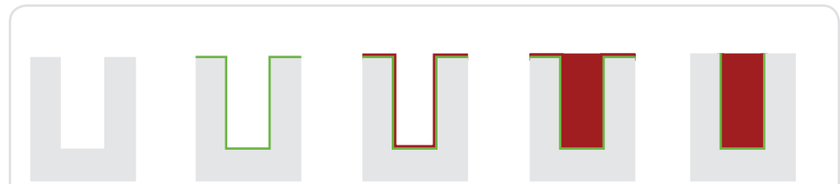


Figure 5. Typical steps in TSV fabrication.

TSVs are being used in applications such as LEDs, power devices, and MEMS to enable low-profile interconnects and as a path toward 3D integration and die-stacking. TSV technology is quickly migrating across application segments to meet the demand for devices that are not only thin but also have small footprints.

This push, once thought to be motivated by the trend toward end-device miniaturization, now is supported by a combination of overall size reduction and the need to free-up space for other critical elements, such as displays and batteries.

The process capabilities needed for TSV production are etch, CVD, PVD, ECD and CMP (see figures 4 and 5).

In 3D architectures extremely thin wafers are needed to facilitate stacking and bonding, on the order of 50µm-thick wafers vs. a standard wafer thickness of 700µm. Without any modifications, existing tools can only handle wafers of ~200µm thickness successfully. Also, process steps such as wet/dry etch and CMP must be handled differently with wafers that are so thin.

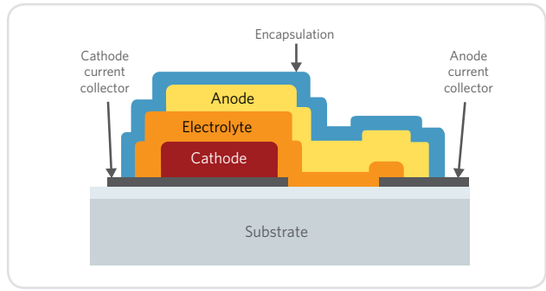


Figure 6. Cross-sectional schematic representation of a solid-state thin-film battery.[2]

THIN-FILM BATTERIES

Implantable medical devices, smart cards, RFID tags, wireless sensors for highly distributed networks, and other electronic products designed for autonomous operation all require power. Solid-state thin-film batteries (TFBs) being developed on 200mm platforms (see figure 6) can open the door to many of these new applications.

TFBs may enable innovations such as power supplies that last the life of a system; distributed power systems consisting of multiple, small form-adhering TFBs; and even near-perpetual energy modules (when combined with energy harvesters). TFBs are also well suited to serve as backup power for memories and microcontrollers.

Solid-state TFBs have technical and performance advantages such as high cycle life (2–3 orders of magnitude higher than conventional Li-ion batteries); a fast charge/discharge rate and near-zero self-discharge rate; high power capability; non-liquid electrolyte; wide operating temperature range; and a

THICK FILMS, NEW PROCESSES, DIFFERENT MATERIALS—

WHAT'S NEXT FOR 200MM PRODUCTION

very thin form factor. This makes them appealing for use in a wide range of applications (see figure 7).

Yet despite their technical advantages and market potential, the transition from R&D to high-volume TFB manufacturing has been slow and challenging. The immaturity of emerging applications is part of the reason, but other major factors include lower energy content (which nevertheless may be suitable for specific application requirements), a higher cost per mAh, and lack of compatibility with high-volume production.

NOVEL MEMS DEVICES

MEMS devices first gained volume production in automotive and printing applications. More recently, growth in consumer applications has spurred the growth of MEMS devices such as gyroscopes, accelerometers, and digital compasses.

MEMS is fertile ground for new technologies, and the integrated pico-projector is one of the potentially high-volume ones. Integrated in smartphones or other mobile devices, pico-projectors are based on an assembly of MEMS micromirrors, with the most recently announced developments using red, green and blue lasers to "write" an image on a rastering micromirror surface.

Stand-alone models currently on the market have limited functionality. As more integrated, brighter, and less power-hungry units become more widely available, they may spur new and innovative uses of this projection technology. Emerging projectors employ MEMS-based technologies capable of targeting device thicknesses of less than 5mm, making them suitable for most contemporary smartphones and portable devices.

MEMS fabrication technologies for the production of next-generation, integrated functionality devices are also under development. One is reduced aspect ratio dependent etch (ARDE). When combining accelerometers or gyroscopes with large-cavity devices such as pressure sensors, a key productivity challenge is to etch large critical dimension (CD) trenches alongside smaller trenches (CD=1µm or less) at the same rate. ARDE promises to make this possible.

Other MEMS processes under development are aimed at process challenges related to material properties; for example, micro-bolometers used in night vision and thermal-imaging systems. In the case of thermal imaging for industrial applications, micro-bolometer film requirements may need tuning beyond what is considered typical in other segments. Specific electrical properties will be needed that may require additional development effort, adding complexity and cost to the manufacturing challenge. Even within a device family, applications may require different categories of MEMS performance.

In the future, as more tangible, everyday objects become embedded with sensors and gain the ability to communicate, the resulting network—which some are calling the "Internet of Things"—will begin to take shape. The Internet of Things will have the potential to quantify almost every aspect of our environment, reducing costs, changing current practices and ultimately impacting our daily lives in countless ways. For example, distributed temperature and flow sensors could be placed on a building's heating/air conditioning vents to monitor total system performance with a degree of precision not currently available except at high cost.

The question is, how will this new class of independent sensors be powered? MEMS technology theoretically could be used in an energy-scavenging role; for example, to convert the mechanical energy of vibration into the tiny amounts of electrical power required to operate the sensors and broadcast sensor readings to a larger network.

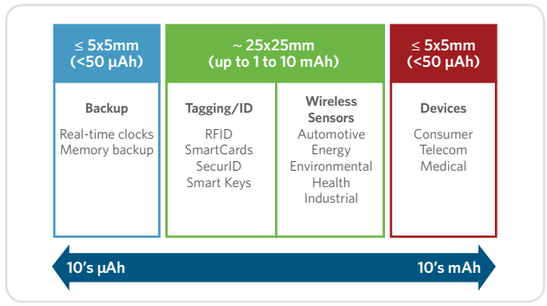


Figure 7. Replacement and emerging applications for thin-film batteries.

THE FUTURE BEGINS NOW

Manufacturing innovative, highly integrated future products will require new technology capabilities such as the ones described in this article. Applied Materials sees 150mm/200mm tools as attractive platforms on which to advance many of these key technologies.

Independently, and in collaboration with customers, Applied continues to invest in process and equipment development that will turn workhorse 200mm tools into enablers of new technologies that will make life easier and better.

For more information, contact mike_rosa@amat.com.

[1] http://www.eetasia.com/ART_8800669970_765245_NT_59f88ef4.HTM

[2] N. J. Dudney, Solid-State Thin-Film Rechargeable Batteries, Materials Science and Engineering B 116 (2005) 245–249, Elsevier.

STRONG ENGINEERING FOUNDATION

SUPPORTS YIELD IMPROVEMENT

Yield is the single largest contributor to the financial performance of a semiconductor fab. Yield loss during a new technology or product ramp costs the industry as a whole billions of dollars annually, or tens of millions of dollars per fab. But in addition to the poor yield results themselves, yield losses impair the rate of learning because scrapped wafers or confounded results require additional learning cycles, thus further contributing to loss in time-to-market and in revenues. A fast learning rate is a requirement for high-achieving fabs.

BY HELEN ARMER

According to Patrick Fernandez, director of Applied Materials' FabVantage Yield Consulting Practice, a large majority of yield loss is due to process and equipment behavior. The remainder is due to device design issues, process integration marginality, manufacturing errors, and facilities problems such as airborne molecular contamination.

Process tools are deterministic: for a given set of process and equipment inputs, the on-wafer result can be derived from engineering or statistical models that are verified with physical understanding. Thus, the majority of yield problems can be solved by fixing issues on the process tools. For example, a fundamental driver of a high density plasma (HDP) process is the deposition-to-sputter ratio. If deposition and sputtering are not optimized, the deposited film can pinch off the entrance to the "gap" (a recessed region that, in cross-section, looks like a via). The result is an incompletely filled gap. This defect, known as voiding, causes electric current leakage, a yield killer. Figure 1 illustrates such a void.

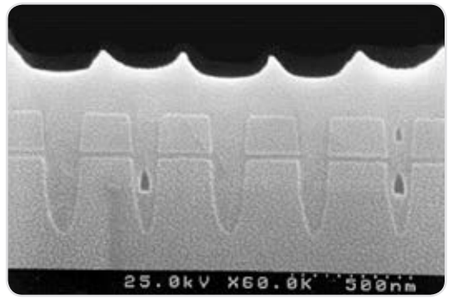
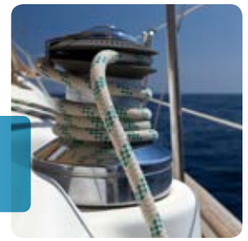


Figure 1. Illustration of a void caused by deposited film pinching off the entrance to the gap in an HDP gapfill process.

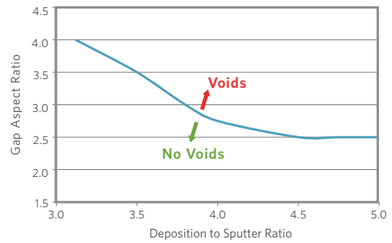
STRONG ENGINEERING FOUNDATION

SUPPORTS YIELD IMPROVEMENT

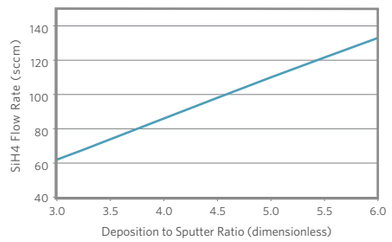


Process and hardware characterization of an Applied Materials HDP chamber identified process regimes that give a void-free gapfill as a function of the structure's aspect ratio (see figure 2a). This model, combined with other process characterization on this chamber, can be used to troubleshoot a void problem. Figure 2b illustrates a second characterization model needed to optimize this process on a given set of hardware.

In all, seven process parameters need to be simultaneously optimized to produce a high-yielding structure. While this example is simplistic, it illustrates the extent of process characterization needed to identify and correct misprocessing on a tool and thereby eliminate yield problems caused by process and equipment.



(2a) Process regime that gives void-free gapfill on HDP chamber.



(2b) Model to tune the process to achieve a target deposition-to-sputter ratio.

Figure 2. Process characterization models for the HDP process.

KNOWLEDGE BUILDS BETTER YIELD FROM BOTTOM UP

Conventional yield improvement methodology is essentially top-down: start with the outputs—low-yield and non-yielding wafers—and attempt to determine which process steps are the root cause. One problem with this approach is that failure is observed at the end of the line (after hundreds of process steps) or much farther down the line, and weeks may have elapsed since the wafer was misprocessed. During this time, the tool could have been changed, such as by doing preventive maintenance (PM), and the problem may have been fixed.

Usually, it is difficult to identify the root cause. Fabs still have the historical statistical process control (SPC) or fault detection (FD) data for the tool, and this is used to perform root cause analysis, but the root cause may remain elusive if the SPC models are not tracking the correct sensors or if the control limits are not correctly set for detecting yield-detracting excursions. Furthermore, traditional SPC and FD models present their own problems related to the large amounts of data collected and acted upon, alarms, and false positives or negatives (see the article "Software Is Key To Effective Yield Management" elsewhere in this issue).

In addition to these top-down methods, the Applied Materials FabVantage consulting group offers this bottom-up approach: ensure that the process and equipment inputs are optimized for the intended result. The bottom-up approach requires a methodology for identifying the suspect processes and equipment, no small task in a fab that contains hundreds of tools running hundreds of process steps. FabVantage uses a rigorous methodology that was developed over many years of experience and builds on our vast tool and process knowledge. Some examples of our methodology are:

- **Benchmark each tool against best-in-class data from our knowledge base.** Benchmarking is used to identify tools with poor defect performance and high unscheduled downtime, both of which flag potential yield loss.
- **Review parametric failure paretos.** These may show manifestations of failures that have previously been documented. For example, high transistor leakage variation is sometimes associated with poor temperature control on rapid thermal processing (RTP) spike anneal tools.
- **Study customer inputs and the history of what they have tried.** Customers can often isolate problems to a few tools or modules based on factors such as chamber mismatch, high downtime, and difficulty recovering tools after maintenance.
- **Review failure paretos and wafer-level metrology data from tools with the most failures.** For example, if a CVD tool is being taken down frequently for faceplate or liquid flow meter issues and we see marginal thickness or thickness uniformity performance, then we have a suspect tool. This tool may be running an unoptimized recipe or it may have incorrect equipment constant settings or hardware setup, or perhaps it is not being properly maintained.

As the above discussion of methodology suggests, the knowledge base is one of the critical capabilities of the FabVantage approach. The Applied knowledge base is our extensive compilation of tool performance metrics and best known methods (BKMs). It contains data on each tool's entitlement for uptime, throughput, process results on the wafer, and particles. It contains BKM recipes, equipment constant settings, maintenance procedures, hardware configurations, and software revisions for >500 kinds of process chambers.

Additionally, the knowledge base contains process trend charts that show process sensitivity to the various controllable inputs and that show regions of process marginality. According to Fernandez, "It is difficult to troubleshoot yield problems without understanding these fundamental drivers. We have seen incorrect recipe or equipment setup that has resulted in many wafers being scrapped."

A common example of faulty equipment setup is incorrectly set mass flow controller verification and correction factors. These can result in flow errors of up to 10% and cause a process to operate on a cliff. Other problems frequently encountered include overcleaning during in-situ cleans, resulting in particle generation; underseasoning, causing a wafer-order effect; and running a process with the throttle valve fully open, preventing pressure control.

Older fabs have the challenge that they are typically operating with legacy tools and processes. They may not have the latest process BKMs or maintenance BKMs and their tools may no longer be set up correctly for the processes that are currently run. Leading-edge fabs face a different challenge. While they typically have new or nearly new equipment, overseen by very capable engineering teams, they often need to operate the tool at the edges of the process window in order to push the device performance envelope. Understanding the process chamber's behavior helps show at what point yield is likely to break down, or where the trade-off between device performance and process stability lies.

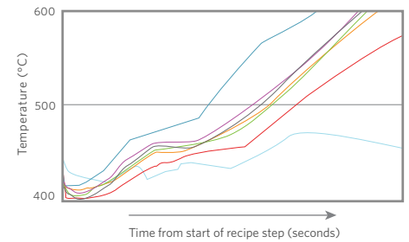
YIELD IMPROVEMENT IN ACTION

The bottom-up methodology discussed above was used in a recent FabVantage customer engagement. A customer was having yield issues resulting in a large gap to world-class yield performance. The yield loss was believed to be associated with new technology introduction, but the root causes were not readily apparent to the customer. FabVantage benchmarking and assessment identified issues related to transistor control and defects. Further, the yield loss was traced to a small set of tools, including RTP. Subsequent detailed assessments of these tools identified faulty equipment, incorrect equipment setup, recipes missing critical steps, and overcleaning during in-situ cleans.

A joint task force between Applied and the customer was formed. The team set inline targets with weekly reviews. A golden tool approach used split lots to verify and qualify improvements. Inline improvements were achieved within three months, and over the following year yield improved significantly.

While a full discussion of the issues found is beyond the scope of this article, the RTP analysis is typical. As a first step toward better RTP performance, the team discovered that the tools' characteristic fingerprints were far from expected baselines, and that process BKMs were not being used. For example, the temperature sensor trace comparison revealed a large temperature variation (far exceeding recommended range) between zones during the temperature ramp up step, as illustrated in figure 3a. This was determined to be the root cause of the substantial within-wafer variation in transistor characteristics reported by the customer.

Resolution of this issue included improvements in maintenance procedures and a recipe change, resulting in a much tighter temperature range during ramp (see figure 3b) and tighter transistor performance. When the root causes were corrected, the temperature spread dropped to the specification of <50°C (see figure 3b).



(3a) Before

(3b) After

Figure 3. Each color in above figures represents one of seven heater zones in the RTP tool. (3a) shows large within-wafer non-uniformity during the RTP ramp. Once BKMs were implemented, the temperature spread dropped significantly to <50°C (3b).

CONCLUSIONS

Yield is the most serious problem affecting fab productivity, and often it is one of the most challenging to solve. However, with the right approach and information, it is also an eminently solvable problem. Fundamentally, yield loss occurs when a tool fails to apply the correct process to a wafer. Though the number of inputs to any given process is large, most semiconductor manufacturing equipment is well characterized. Systematized knowledge, rigorous audit and analysis methodologies, and deep tool expertise can bring dramatic yield improvement results.

Special thanks to Katherine Derbyshire and Patrick Fernandez for their invaluable support in the preparation of this article.

For additional information, contact helen_armer@amat.com

SOFTWARE IS KEY
TO EFFECTIVE YIELD MANAGEMENT

BY SCOTT WATSON

Today's advanced IC manufacturers are collecting more data than they are able to manage effectively. Our discussions with leading semiconductor manufacturers indicate that more than 90% of data is not accessed after it is initially processed during data collection. And the volume of this data is growing exponentially, driven by the improved computing and communication capabilities of tool platforms and expansion in the number and type of sensors installed on advanced chambers.

Forward-thinking manufacturers see this deluge of data as a huge untapped opportunity to proactively improve yield, one of the largest contributors to a fab's profitability.

Effective data management can help fab managers identify yield excursions, initiate root-cause analyses and provide predictive feedback to equipment engineering systems (EES) in order to improve yield.

Statistical process control (SPC) or fault detection (FD) systems are the current standard methodologies used to process data as it is being collected in order to identify yield excursions. Both are valid methodologies, but may not always be applied appropriately. SPC and FD normally utilize statistical control limits that are derived based on the inline process parameters at the specific process step or tool to center the process. Yield excursions—which are shifts in device performance as measured at the end of the line—can still occur even though SPC or FD determine that the inline process parameters are in control.

Leading-edge device makers often have tens of thousands of SPC charts and thousands of FD models. FD is still relatively immature in most fabs but the number of FD models is growing rapidly, so it is reasonable to expect they will soon exceed the number of SPC charts.

However, the sheer volume of SPC charts and FD models is simply impossible to monitor. Too many exceptions would be flagged each day, well beyond the ability of an engineering team to handle manually. Coupled with the fact that these exceptions now need to be tied to end-of-line yield data, the challenge is huge. As a result, the engineering response becomes ad hoc and may or may not address major yield problems. Not only does this waste engineering time, it slows the progress for real yield improvements.

To achieve optimum yields, manufacturers must move from excursion control based on SPC and FD to an overall total yield control solution that leverages high-performance automation to handle large volume data processing. They must also utilize advanced data mining and modeling, and move to yield-driven control methodologies.

Yield-driven control augments traditional process control (SPC and FD) by correlating end-of-line yield data (device performance) with inline process data. Instead of process control based on process centering, control limits for the inline process control are modified to optimize end-of-line yield results, which could be different than process centering.

Applied Materials' FabVantage consulting team recently used yield-driven methodology vs. SPC and FD to resolve yield issues for a 300mm customer. Even though the inline process data was in control for a specific process step, there was a yield problem. Inline measurements were not identifying the cause of the yield variance.

Advanced analysis techniques, including analysis of variance (ANOVA), clearly showed that the problem originated at specific chambers within a specific process step. The inline process data did not show a statistically significant variation between chambers but did show a statistically significant difference in the resulting device performance, which in turn resulted in yield loss. However, the customer was unable to determine the cause of the variation in device performance results across the chambers. A more automated process-driven methodology was required because leading-edge device complexity has so many parameters affecting yield that very sophisticated methodologies must be used to interpret the results.

Applied's FabVantage consulting team initiated a project to assess the situation and identify a solution. Detailed data mining was done on a variety of measurements across the suspect chambers (see figure 1). The analysis showed that certain chambers exhibited much larger variability in I_{drive} performance—resulting in yield loss—even though all the inline process parameters were within control limits. For example in figure 1, the "green" chambers show that most of the results are outside of acceptable I_{drive} performance (gray shaded box) yet the inline process data was all within control.

This analysis identified chambers with the highest yield variability, as well as process steps that were the most closely linked to these yield variations. A subsequent analysis using Applied's E3 equipment engineering system and extensive knowledge base, plus commercial statistical analysis packages and proprietary software and models, enabled the FabVantage team to identify potential root causes. A further analysis "weighted" each item, enabling identification of the most likely root cause.

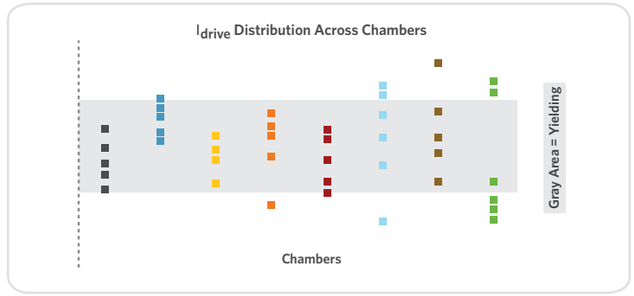


Figure 1. I_{drive} variability across process chambers. All chamber process parameters are within spec for inline process control, yet yield failures are seen (all data points outside shaded box above do not yield).

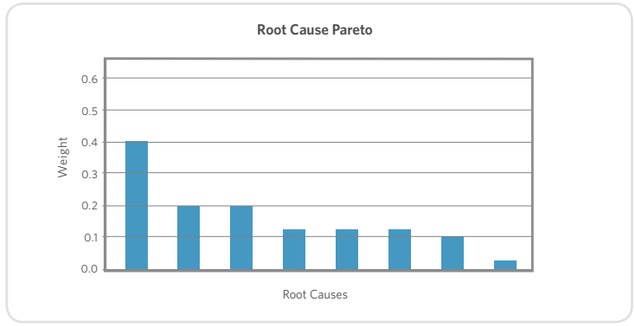


Figure 2. Use of analytical tools and data mining provide pareto of potential root causes of yield variation.

SOFTWARE IS KEY
TO EFFECTIVE YIELD MANAGEMENT

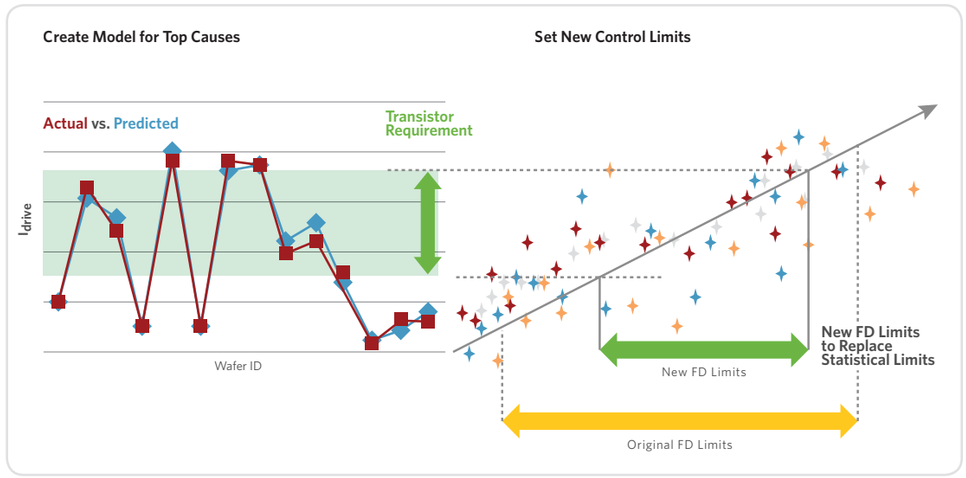


Figure 3. Models that predict I_{drive} are correlated to FD limits and yield. Such yield-driven control limits are often different than locally optimized inline process FD limits.

These root causes will typically be a combination of critical chamber sensors, tool constants, and recipe parameters. The results allowed the FabVantage team to model these top causes of yield variation and set new inline yield-driven control limits that were derived from the yield results versus inline statistical control limits (see figure 3). The transistor requirement (green arrow) identifies the range that ensures good yield.

The team created a model of the root cause sources to the expected resulting transistor requirement. This model is then used to derive new inline process control limits that will control the resulting yield performance. These changes were implemented on a "golden tool" and successfully qualified by the customer. The changes are now being deployed across the remaining chambers.

The key to all this is software—software that can collect the requisite data, support the data mining activities to derive the root causes, model the root causes to inline tool performance parameters, and establish yield-driven control limits. In the previous example, FabVantage used a variety of software solutions to derive results as listed below:

- **Applied E3 equipment engineering system:** High speed/high volume chamber sensor data collection, trace analysis and data mining.
- **Commercial statistical analysis packages:** SAS, JMP, Spotfire and others utilized for additional yield analysis, modeling and data mining.
- **Proprietary software/models:** Models developed by the FabVantage team to augment E3 and commercial software packages.
- **FabVantage Knowledge Base:** Capture of a wide range of critical yield/process information and best known methods to facilitate root cause analysis.

In order to implement yield-driven control limits, it is also crucial to analyze the equipment constants across the tools to identify variability that could impact yield performance. In the example above, this was done manually. However, this represents another opportunity to apply software to automate the comparison of key equipment constants.

With the rapid growth in the amount of data being collected and as yield issues for advanced technology nodes become more challenging, it will become critical to automate this yield methodology. Such a solution will enable manufacturers to correlate yield and device performance excursions to key tool performance parameters and establish specific FD models to improve yield.

Applied calls its methodology for implementing this automation solution enhanced advanced process control (YMeAPC). It integrates equipment control (FD) with yield management system (YMS) and equipment engineering system (EES) capabilities in order to improve yield and reduce cost. Implementation of this capability will further automate the yield-driven control methodology described in the example above and enable automatic modification of limits as yield performance correlations change over time.

Figure 4 shows an overview of the YMeAPC concept. It leverages an equipment automation layer that is typically already provided with an EES deployment. It includes collections of data from equipment (settings), the manufacturing process (variables) and the product (metrology, e-test) in real time as necessary to support capabilities such as FD control.

A subset of the equipment automation data is summarized by the FD system and then is correlated with yield information from e-test and yield metrology to derive a total yield-prediction capability.

This yield-assessment and -prediction capability serves as a crucial early-warning system. It can enhance productivity by providing yield information to critical functions, including maintenance, scheduling and dispatching, and run-to-run control, enhancing decision-making and yield optimization.

This collaborative and flexible integration is achieved by an event-driven strategy engine. All communications between components (arrows) leverage standards wherever possible to maximize interoperability and the interchangeability of components.

Although the YMeAPC framework begins to take advantage of the vast amount of data being captured by IC manufacturers, there are further opportunities to leverage it. Because a significant number of yield surprises are caused by events known to impact yield that go unobserved, there is an opportunity to use advanced data-mining and modeling techniques to analyze the massive volumes of data in a background mode to identify and prioritize the source of yield variances.

This modeling can employ standard statistical methods such as ANOVA to provide ongoing reports of potential causes of yield variance, which then can be used by process and yield engineers to prioritize their work. Ideally, these models initially would be established as part of the technology integration process so they can accompany new process introduction into the wafer fabs. Over time, they can be optimized in order to improve the results. The key is to consistently utilize this untapped data.

Moreover, as EES solutions advance, these capabilities will become integrated as standard models for transforming current tool control methods and practices into more automated, advanced yield control.

Special thanks to Dr. James Moyne and Patrick Fernandez for their assistance in creating this article.

For additional information, contact scott_watson@amat.com

Additional reading on this subject:

J. Moyne, B. Schulze, "Yield Management Enhanced Advanced Process Control System (YMeAPC): Part I, Description and Case Study of Feedback for Optimized Multi-process Control," IEEE Transactions on Semiconductor Manufacturing, Special Issue on Advanced Process Control, *Vol. 23, No. 2, (May 2010), pp. 221-235.*

J. Moyne, N. Ward, R. Stafford, B. Schulze "Yield Management Enhanced Advanced Process Control (YMeAPC)," (Invited session keynote), International SEMATECH AEC/APC Symposium XX, *Salt Lake City, UT, (October 2008).*

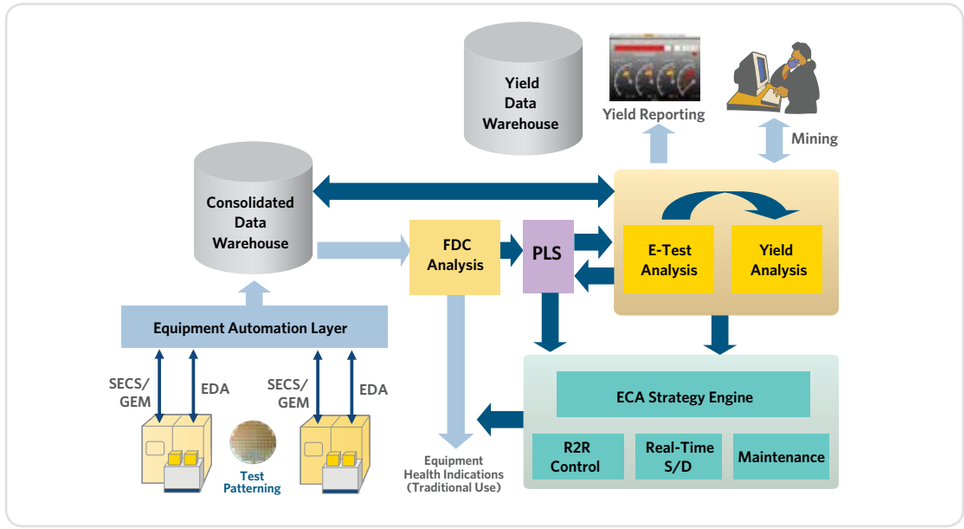


Figure 4. High-level view of YMeAPC solution.

A Customer Story

SPANSION

WRINGS HIGHER PRODUCTIVITY, LOWER COSTS FROM 200MM FAB

BY DAVID LAMMERS

No fab can remain static for long in today's competitive world, and older fabs require just as much innovation and creativity to remain competitive as the leading-edge fabs—perhaps more so.

Worldwide more than a third of the wafers processed this year will be 200mm in diameter, according to market research firm IHS iSuppli, to make a wide variety of products, including analog and power ICs, sensors and MEMS. Europe, with its strength in automotive ICs and sensors, is a major 200mm center.

Among the world's 200mm fabs, Spansion's flash memory operation in Austin, Texas, has remained particularly dynamic. Spansion is among the many companies coaxing higher productivity and lower costs from 200mm fabs.

Not far from Spansion's fab, Freescale Semiconductor makes microprocessors and MEMS at two 200mm facilities. In nearby San Antonio, Texas, Maxim relies on its 200mm facility to make its leading analog products. These are just a few examples of large semiconductor companies relying on 200mm fabs for the majority of their revenues.

Spansion became independent of Advanced Micro Devices at the end of 2005. The perils of supplying NOR flash to the cyclical cell phone market and an unsuccessful effort to build a state-of-the-art 300mm fab in Japan led the company to a Chapter 11 bankruptcy reorganization in March 2009. It emerged from Chapter 11 in May 2010 and now has annual revenues of roughly a billion dollars.

The new management team, led by CEO John Kispert, recognized that the 200mm Fab 25 in Austin was fully depreciated and able to profitably make the chips that became Spansion's bread and butter: highly differentiated "embedded flash" solutions sold to some 7,000 different customers.

Fab 25 may be unique in that it can manufacture at 110nm, 90nm, and 65nm simultaneously, with an aluminum back end for the 110nm devices and copper interconnects for the 90 and 65nm products. When demand exceeds Fab 25's capacity of 40,000 wafers per month, the company relies on foundry partner SMIC for some 65nm production needs.

FINDING YIELD KILLERS

To meet high demand and achieve profitability goals, Fab 25 director of Engineering Gary Dawson said his team has worked to wring every last ounce of productivity from its 200mm tools. "Through many iterations of learning we have developed this factory to be the ultimate in flexibility." The Spansion factory is packed with equipment and any increases in production volume must come from making the existing equipment and space more efficient and productive. That is where a series of Applied FabVantage consulting engagements came into play.

Dawson said one of Spansion's challenges with its 200mm equipment "is not so much base functionality, but defect performance. A very large improvement as the industry went to 300mm from 200mm is in the ability to process wafers more cleanly," he said. The defect challenges come partly from the wafer handling equipment, with chamber design also playing a role.

Gary Dawson, director of engineering, Fab 25, Spansion, Inc.

SPANSION
WRINGS HIGHER PRODUCTIVITY, LOWER COSTS FROM 200MM FAB

To help reduce defects and boost throughputs, Spansion engaged with Applied's FabVantage consultants for three separate projects, one each on Mirra Mesa CMP, DPS metal etch, and Producer dielectric deposition tool sets. While each project was different, Dawson said the three engagements all involved bringing in a small team of FabVantage consultants to audit Spansion's maintenance and processing methods. Spansion would ask that the effort meet certain objectives, such as reducing defectivity by 50%, or improving throughput by 10–20%, depending on the tool.

The most successful engagement, Dawson said, involved an effort to improve the throughput of the Producer dielectric deposition equipment. "Applied brought in five guys, and they did an industrial engineering analysis of how wafers are queued up and staged, with different timing scenarios within the tool. They made recommendations, we made those tweaks, and we got what we wanted: a 20% throughput improvement and 2% to 5% better uptime."

Avoiding unscheduled down time—part of an effort to improve what Dawson calls the "variability of availability"—is a prime focus of the fab engineering team. For DPS metal etch, Dawson said Spansion's etch team contacted Applied and said they wanted to improve the variability of availability by 50%, as well as a 50% reduction in defects.

The Applied consulting teams observed teardowns of the etch equipment, how it was cleaned, reassembled, and brought back into service. They examined preventive maintenance (PM) techniques, and the way the process is run, including how the plasma is struck, gas flows, and pressure. They compared what they saw against Applied's best known methods (BKMs) and made remedial recommendations.

"After we discussed the BKMs with the FabVantage team, we did another PM, invoking the recommended changes, and monitored for improvements," Dawson said. He noted that the collaboration is still in progress, with final outcomes yet to be determined.

"One of the attractive things about Applied Materials is that it has done a really good job of evolving 300mm equipment improvements, and then back-introducing them into 200mm equipment," Dawson said. The FabVantage engagements allow Spansion to take "full advantage of not just the hardware improvements, but procedural issues and BKMs," he said.

KEEPING IT PRODUCTIVE

In addition to looking for continuous improvement and new applications for 200mm systems, integrated device manufacturers (IDMs) with "More than Moore" fabs are increasingly concerned that with so much focus on 300mm, and soon 450mm, support for replacement parts and services on older tools will wane.

With such concerns in mind Spansion set up its own repair shop in 2008, and has expanded its ability to repair boards, re-creating some parts where needed. "We have become more self-sufficient, improving our ability to survive," Dawson said. "We do more with less, and when it makes sense we try to do more things internally."

For example, Dawson said some of AMD's skills at advanced process control (APC) were refined by in-house teams as Fab 25 passed into Spansion's possession. APC allows on-the-fly adjustments; for example, if a lot is found to be outside of a statistical distribution, the equipment can be stopped in real time for adjustments to improve yield and performance. Fault detection is widely used to gauge equipment performance.

Also, the company's engineering team has developed "Lot Dossier," an application that provides real-time feedback on yields, and a software tool dubbed Pluto that supports changes to the mix of work in progress (WIP) as customers request more of a certain product.

LOOKING FORWARD

The next big push for Spansion? Predictive maintenance (PdM), aimed at extending the time critical parts can be kept in service. "Again, certain aspects of the PdM program will be done collaboratively with Applied, while key algorithms will be closely guarded as our proprietary information," Dawson said. PdM is all part of improving the "variability of availability" that Dawson's team is so focused on, which in turn is part of a "kaizen" attitude of seeking continuous improvement.

In addition to sharing benchmarking data with ISMI and the Fab Owners Association, Dawson said that internal controls are critical as well. "Part of our kaizen process is that we monitor ourselves obsessively, on a daily, weekly, and quarterly basis," he said.

For additional information about Spansion visit www.spansion.com

200MM— ALIVE AND WELL?

Jim Scholhamer, general manager of the Components and Systems Group at Applied Global Services, said the 200mm business is indeed alive and well, with about 12,000 Applied 200mm tools out in the field, many of them still working after 20 years in operation. And the 200mm tools keep getting better. "We have an engineering team dedicated to 200mm equipment upgrades and enhancements," he said. For example, advances in power supplies and multi-zone CMP polishing heads originally introduced in 300mm generation tools have been brought back into 200mm equipment.

Scholhamer said that Applied Materials recognizes there is a lot of the company's 200mm equipment out in the field and that it is "not fading away and dying." With the power ICs, automotive sensors, and MEMS markets growing, Applied is continuing its efforts in refurbished and, in some cases, new 200mm tools. In addition to its own manufacturing and continuing investments in 200mm application development, Applied has forged relationships with qualified, specialized used equipment suppliers to support customers.

Asked about obsolescence of key parts, Scholhamer said a dedicated team is in place to handle that area. In addition to qualifying some specialized part vendors, the team uses modern technologies to re-engineer OEM parts that are no longer available. "There are some things we just can't outsource," he said.

Beyond the technical challenges, the 200mm equipment market represents unique business challenges. "Unlike 300mm, at 200mm the deals are large in number and of relatively small size and it creates a challenging market to address," Scholhamer said. Demand shot up in 2010, and while the market has eased back in the last two years, it continues to be "a pretty robust and healthy market."

REAL-TIME DISPATCHING OPTIMIZES SEMICONDUCTOR PACKAGE ASSEMBLY

BY DAVID HANNY

Complexities in semiconductor packaging assembly have increased significantly over the years, challenging on-time delivery and cost performance.

In particular, the wire bonding step is a common bottleneck in assembly operations,[1] where its manufacturing efficiency directly affects on-time customer delivery. A medium-sized or larger assembly facility generally has hundreds if not thousands of wire bond machines. Product lots typically spend more processing time in wire bond than in any other assembly operation because of the growing complexity of packages and the increasing number of lead and wire counts.

Additional operational challenges stem from increasingly shorter product lifecycles, growth in product mix, and the movement to outsourced assembly and test services (OSATs) where multiple packaging technologies must coexist in the same factory. These factors contribute to growing costs in semiconductor back-end operations.

The major challenges arising from these factors generally fall into four main categories: capacity imbalances, management of equipment setups, manufacturing data management, and factory dynamics.

1. **Capability imbalances** occur because the growing diversity of assembly equipment has brought varying degrees of both automation and capabilities to handle different product types, wire/pad pitches, and wire types and sizes. When equipment disparities are not well understood, operational planning is suboptimum and shop-floor performance suffers. One major integrated device manufacturer (IDM) has reported that capability imbalances alone led to a 13% drop in wire bond tool utilization (68% actual utilization vs. 81% planned utilization).[2]
2. **Wire bond setup** has become complex, tedious, and iterative, and thus the management of setups and product changeovers greatly affects productivity. Success on the first pass is the goal but in reality several attempts are needed, causing long setup times and significant technician involvement. This results in wasted production time at the bottleneck and lost product (because units are consumed during setup). Further, manufacturing effectiveness is negatively impacted due to unplanned setups, product priority changes, quality problems, unscheduled equipment downtime, and improper product routing.
3. **Manufacturing-related data** is becoming complex and now is gathered from many sources, such as manufacturing execution systems (MES), product and equipment engineering systems, and enterprise resource planning (ERP) systems. This makes it challenging to quickly gather all needed data for timely decisions. Relying on shortcuts such as examining process data less frequently or using stale data can diminish the ability to deliver the right quantity of product on time.
4. **The influence of factory dynamics** should not be understated. Even when good plans are developed, good execution mechanisms are in place and data is aggregated effectively from multiple sources, productivity suffers when operational adjustments are not properly executed. This has been observed in scenarios such as product holds, equipment downs, product priority changes, and when peripheral resources like paddles and clamps are unavailable.

Add it all up, and short predictable cycle times are becoming more and more difficult. This in turn results in a reduced ability to deliver shipments to customers on time.

DISPATCHING REQUIREMENTS

In the past, human decision-making alone was adequate to manage and operate semiconductor packaging assembly operations. But today's challenges, coupled with the growth of networked production environments, dictate the need for timely, accurate, consistent, and scalable data-driven solutions to support operational decision-making.

Rule-based real-time dispatching is one such solution that has enabled factories to improve performance for on-time customer delivery, work-in-progress (WIP) cycle time, and product output. Dispatching can be defined as the setting and initiation of production activities and instructions in accordance with factory objectives such as on-time delivery, cycle time, bottleneck utilization, etc. Its goal is essentially to get the right product to the right equipment at the right time, a capability typically beyond what an MES is capable of doing.

Dispatching solutions must be seamless, execute quickly, use aggregated real-time data, capture business rules easily and provide useful information to all manufacturing stakeholders.

As shown in table 1, effective solutions must support such critical requirements as:

- **Reporting and business rules representation.** A successful planning and scheduling solution must provide planners with data management/transformation functions so they can create weekly, daily, or even per-shift plans. These functions must have access to real-time data so that operational changes can be made nimbly as needed.
- **Dispatching and scheduling execution.** Once a good plan is created, a means to execute to it must be provided. The solution must be systematic and not prone to human-introduced errors; thus it must be integrated with factory MES transactions so that the same business logic used to generate plans is used in dispatching and scheduling. Shop-floor and equipment-specific considerations must be incorporated to balance factory objectives with practical operating constraints.
- **Real-time data access and representation.** Real-time data is crucial. Without it, decisions are less effective and the planning and scheduling functions are less credible. When people don't trust the system they tend to circumvent it, which leads to higher manufacturing variability and poor planning execution.
- **Effective change management.** Many good planning and scheduling solutions fail because they are implemented as add-ons to existing business processes. A successful solution must minimally disrupt business processes and shop-floor end users. It also must easily handle changes in business logic and data sources without complex coding, and allow production engineers to define and manage the business logic representation.
- **Compliance-monitoring.** Even the best planning and scheduling solution can't be effective if it isn't used. Therefore a successful solution will enable decision-makers to monitor its usage. The ability to measure operator compliance with automation decisions enables timely corrections and better planning. For example, when operators don't follow dispatch decisions it may indicate that there are inherent flaws in the business logic.

Required Capabilities for Achieving Enhanced Factory Performance
Reporting and business rules representation
Dispatching and scheduling execution
Real-time data access and representation
Change management
Compliance monitoring

Table 1. Summary of required dispatching capabilities to achieve enhanced factory performance.

DISPATCHING SOLUTION INCREASES ASSEMBLY PRODUCTIVITY

Let's take a closer look at a high-volume OSAT manufacturer's assembly operation.

The factory experienced a high degree of variability for both products and processes. This was impacting their ability to deliver products on time to their customers. A deep dive into the customer delivery dilemma uncovered a manufacturing problem at the wire bond step, wherein the wire bonders (the factory-designed bottleneck) were exceeding their planned idle time and also were exceeding the number of setups, hindering the ability to meet throughput goals.

With thousands of wire bonders, the problem was impacting overall production and had a particularly adverse impact on high-priority lots. Additionally, although the process at the wire bond step required highly capable operators with great expertise, there were time lags in making key manufacturing decisions. Digging deeper into the manufacturing challenges, it was discovered that the decision-making process regarding what to process next was unclear and poorly defined. The result? Inconsistent operator behavior, poor loading/unloading time, and unpredictable results.

The OSAT manufacturer determined that to resolve this challenge, it was necessary to standardize and automate their process at this bottleneck step. The expectation was that if this key process was automated, it would enable an increase in wire bonder utilization and a decrease in process variability, thereby creating a more predictable factory. The OSAT manufacturer selected Applied's APF Real Time Dispatcher (RTD) software for the project.

Manufacturing execution data was captured from multiple sources. These event-driven updates allow the dispatching system to continually make decisions with the current state of the factory, including process step completion, WIP on hold, and equipment down.

REAL-TIME DISPATCHING

OPTIMIZES SEMICONDUCTOR PACKAGE ASSEMBLY

Further, because order fulfillment priorities were changing as customers made frequent updates to their orders, best practices for operators were developed to determine which lot to process next, creating execution logic at the wire bond step. For example, tool allocation reports are executed in order to provide the latest status of available equipment. As equipment is ready for the next WIP, a "what-next" logic is executed, which in real-time determines what WIP is being processed, taking into account factory dynamics. This logic considers the latest WIP location and expected arrival times of future WIP.

On the shop floor, operators were trained on the new procedure, and compliance reports were used to verify adherence to the manufacturing process changes.

MANUFACTURING RESULTS

The results reported were very favorable. They are categorized as shown in table 2.

Results
Equipment: measured between 5–10% OEE improvement
• Reduced tool idle time • Reduced tool set up / change over time – Increased train size – Reduced cycle time
WIP KPI
• Reduced hot-lot cycle time • Improved on-time delivery
Human effort KPI: 30% reduction in operator workload
• Significantly reduced expertise requirements for operators • Significantly reduced the training time required for new operators • Enabled new operators to be assimilated quickly into manufacturing • Significantly reduced human loading for material push • Significantly reduced human loading to follow up lot (hot-lot)
Management
• Provided transparent and real-time information for production control personnel • Provided resource allocation in advance to forecast change-over per shift

Table 2. Results in assembly using RTD.

ABOUT APPLIED APF REAL TIME DISPATCHER/REPORTER

Meeting the disparate requirements for semiconductor assembly, test, and packaging is critical to success in today's fast-moving, ultra-competitive markets. The leading commercially available solution specifically designed to meet these challenges is APF RTD and APF Reporter from Applied Materials. Deployed in more than 200 production facilities globally, it is a real-time, high-performance dispatching and reporting system. RTD enables manufacturers to make better-informed and more consistent dispatching/scheduling decisions in order to improve productivity across the assembly and test facilities.

APF RTD and Reporter directs prestaging, releases lots, and adjusts load-balancing of production equipment through "what next, where next, and when next" rules that improve performance of product, carrier, equipment, and labor, with minimal load impact on MES performance. It helps manufacturers identify and implement process improvements without complex application programming, and provides reporting tools for analyzing manufacturing data and identifying key constraints and areas for improvement.

CONCLUSION

Applied RTD and Reporter offers semiconductor assembly, test and package customers the opportunity to enhance their planning and scheduling functions. It is designed for their unique manufacturing needs: real-time data access, rules-based dispatching, real-time reporting, and scheduling for reacting to changes as they occur. Production planners are using the reporting and dispatch capabilities of RTD to optimize the daily production and customer delivery plans. These plans are then driven to execution through dispatch decisions that also improve asset utilization, enabling greater returns on investment and profitability. Developed and deployed at over 200 factories worldwide, RTD has incorporated these unique requirements into an out-of-the-box solution that has successfully demonstrated bottleneck capacity expansion and cycle time improvements. Production planners using RTD have optimized dispatch decisions and improved asset utilization, driving greater returns on investment and profitability.

For additional information, contact: david_hanny@amat.com or shekar_krishnaswamy@amat.com

[1] *Daniel Quadt, Simulation-Based Scheduling of Parallel Wire-Bonders with Limited Clamp & Paddles, Proceedings of the 2006 Winter Simulation Conference, Perrone, Wieland, Liu, Lawson, Nicol and Fujimoto. Eds.*

[2] *Alvin Y. Fong, An Assignment Model in Optimizing Wire Bond Total Utilization in Multiple Tool Type and Product Mix Environment, Proceedings of the International MultiConference of Engineers and Computer Scientists 2008 Vol II, IMECS 2008, 19-21 March 2008, Hong Kong*

Additional Reading

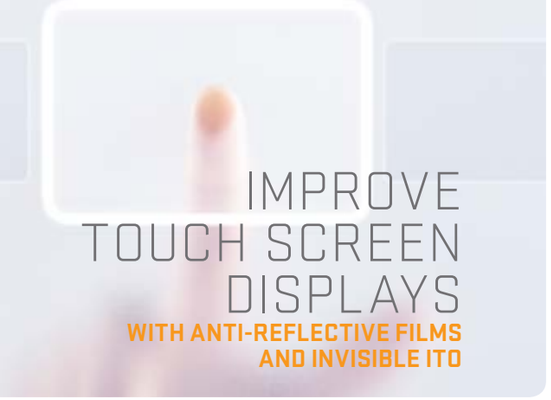
Bala Iyer & Binay Dash, Real Time Dispatching—A Catalyst to Assembly Test Manufacturing Execution Automation, Proceedings of the 2011 Winter Simulation Conference, Jain, Creasey, Himmelspach, White & Fu. Eds.

IMPROVE TOUCH SCREEN DISPLAYS

WITH ANTI-REFLECTIVE FILMS AND INVISIBLE ITO*

Touch panel technology is one of the most exciting developments in displays, with smartphones and tablet PCs representing the most prolific applications for the technology. Touch interfaces are an enabling technology for the mobile display market, which accounts for sales of about 100 million tablets and 690 million smartphones. Today more than 40% of smartphones use touch panels, and this is expected to surpass 50% of mobile phones by 2014.[1]

** invisible indium tin oxide*



IMPROVE TOUCH SCREEN DISPLAYS

WITH ANTI-REFLECTIVE FILMS AND INVISIBLE ITO

INTRODUCTION

More than a dozen touch screen technologies exist, including projected capacitive, surface capacitive, resistive, on-cell, infrared, optical touch, acoustic wave, digitizer, and others. However, in small/medium displays such as phones and tablets, capacitive touch has emerged as the clear leader because of its form factor, reliability and multi-touch capability. Multi-touch refers to a touch screen's ability to recognize the presence of two or more points of contact with the surface. A good example of this is when you are using two fingers on the touch screen at once to pinch a photograph to zoom in and enlarge it.

In general terms, capacitive touch works by having two layers of transparent conductor patterned into an X-Y cross-pattern. The two layers are separated by an insulator of glass, or deposited thin film. When a finger touches the screen, its electric field is distorted. The location of the distortion is sent to the controller for processing. In the "one glass" solution shown in figure 1, the X-Y ITO layers are deposited in one layer, eliminating one layer of glass to reduce manufacturing costs.

A capacitive touch panel film stack may have 15+ film layers, and most of these stacks require 4–5 physical vapor deposition (PVD) layers. Some of the layers, such as anti-reflective (ARC) coatings and invisible indium tin oxide (ITO) electrodes, are there to improve the user's perceived viewing experience and thus are unique to touch panels.

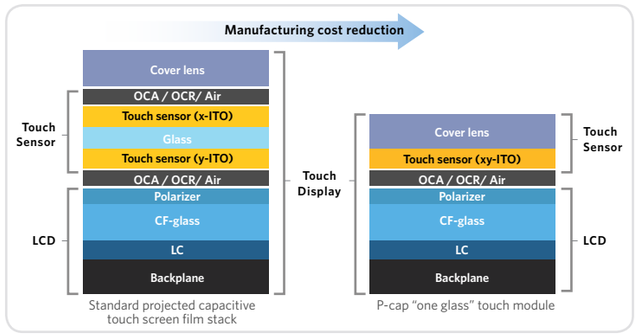


Figure 1. Examples of projected capacitive touch screen integration schemes.

Anti-reflective, color-neutral coatings enhance sunlight readability and increase display brightness by reducing the visual reflectance on the substrate surface; for example, on the cover lens outer surface. Invisible ITO electrodes in the layer stack, meanwhile, offer pattern invisibility, enhanced color-fastness, increased transmittance, and reduced reflectance.

DISCUSSION

Thomas Zilbauer, Applied's project manager of R&D for PVD Display Engineering, has been developing invisible ITO and ARC films at Applied Materials in Alzenau, Germany for the past two years. He spoke recently with Kerry Cunningham, product marketing manager in Applied's Display Group.

Q. Thomas, do consumers enjoy an enhanced visual experience from invisible ITO in touch panel-capable devices?

A. Invisible ITO targets enhanced optical performance, enabling the user to experience brighter displays, more colorfast displays, and displays without any distracting sensor patterns. With regard to the latter, in most of today's smaller mobile phones the touch sensor patterns are barely visible if at all in off-mode under sunlight reflectance. When they are visible they can generate complaints from people who see them and worry needlessly that they may have received a low-quality device. But as larger, thinner devices with reflectance reductions for improved sunlight readability fill the market, the conventional ITO pattern becomes increasingly visible and results in distracting patterns even during display operation. Invisible ITO then becomes an inevitable necessity.

Q. Do the invisible ITO and anti-reflective coatings support the competing technologies in touch panel?

A. Yes. Anti-reflective coatings are helpful in all 12 major touch technologies, although projected capacitive touch is the main one. Projected capacitive touch is found in approximately 90% of all touch devices given its multi-touch capability, manufacturability and smooth touch operation even in harsh environmental conditions. Invisible ITO supports all technology concept variations of this mainstream technology, whether the touch screen is placed in or on top of the displays. In addition, it enables that technology to be scaled to devices with 30-inch or larger displays.

Q. How do invisible ITO and anti-reflective coatings work, in layman's terms?

A. Both technologies utilize the wave-like nature of light. The thin-film stacks are designed and integrated in such a way that each layer alters both reflected light as well as the light passing through it. Working in concert, the layers have the combined effect of changing the display's overall visual appearance as desired. In the case of anti-reflective coatings, such cooperation among the layers is called destructive interference, which means the reflected light's intensity is decreased in the visual range. In the case of invisible ITO, the film stacks are designed to achieve a light interference that produces a miniscule visual difference between the zones with conductive ITO and without conductive ITO. This difference is indistinguishable to the human eye, both in intensity and hue. (See figure 2.)

However, to achieve these results both the stack design and film deposition require a lot of care. An analogy might be an orchestra, where all contributing instruments must be well tuned to give a pleasant sound. Similarly, the thin films need to be very precisely manufactured. For example, when our customers use one huge glass sheet to produce many phones, the film thickness is allowed to vary only by a few atoms across the entire utilized substrate area, which is as large as 1.1 x 1.3 m^2.

Q. How fast are these technologies being adopted and what are the key advantages for our customers?

A. I am impressed with the adoption of invisible ITO for touch sensors on glass. Leveraging our in-house expertise on the original invisible ITO concept from our SmartWeb technology (roll-to-roll deposition on PET), we could quickly consult with our customers on this material. We have continued to do so as the solutions have gotten increasingly difficult and demanding. Our customers are aware of our expertise in customized stack solutions that address performance, as well as manufacturing robustness for larger yield. Additionally, our rotary magnetron sputtering approach and the process portfolio we have developed are designed for cost-effective deposition of highly demanding optical enhancement coatings.

These anti-reflective and invisible ITO solutions are offered on the Applied Materials Aristo platform, enabling touch screen manufacturers to further enhance the product portfolio for high-performance touch screen products and scale them to larger sizes. The Aristo Twin system and its wide range of process solutions represent the state of the art in touch screen panel manufacturing, making possible sunlight readability, improved color appearance, and clearer touch screens that enhance the user experience.

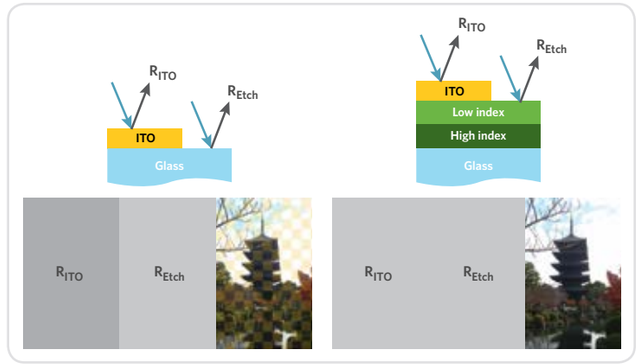


Figure 2. Invisible ITO for projective capacitive touch screen technology. Good index-matching is possible with thin ITO layers, resulting in the ability to produce "invisible" ITO electrodes. R_{ITO} (reflectance of ITO) and R_{Etch} (reflectance of etched area) refer to the fact that the ITO is partially etched for patterning, and in the etched area the structures become visible. There is a difference in the reflection of the ITO layer compared to the etched sections, and a key property for the ITO layer stack is the invisibility of the etched structures, both in transmission and reflection, for a uniform visual experience.

For additional information, contact kerry_cunningham@amat.com

[1] *Internal Applied Materials data.*

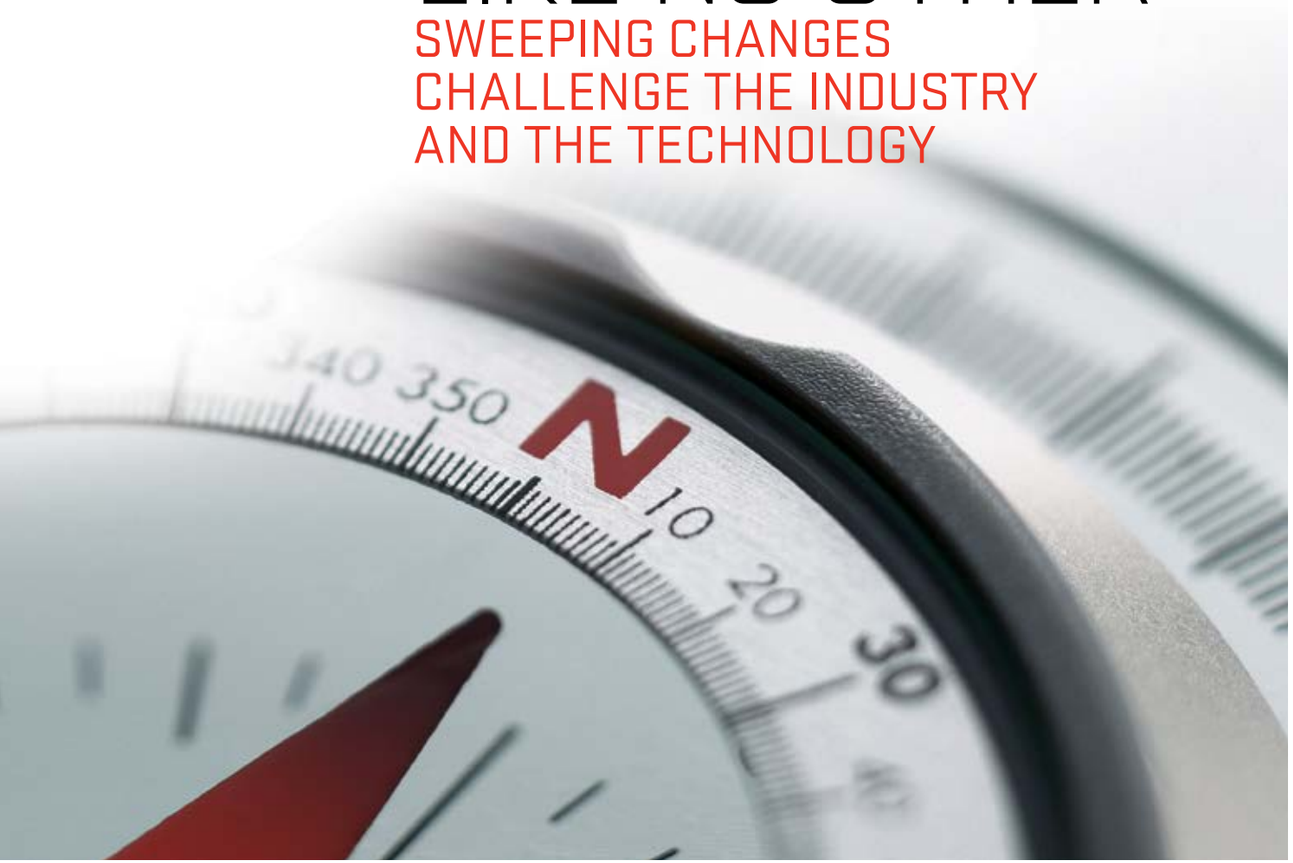
Dr. Thomas Zilbauer, project manager, R&D PVD Display, Applied Materials

ABOUT DR. THOMAS ZILBAUER

Thomas Zilbauer earned a Ph.D in electrical engineering from the University of German Federal Armed Forces, where he developed ALD processes and equipment for high-k based CMOS technology. He joined Applied Materials in 2010 and now is part of Applied's PVD Display group in charge of touch screen technology, roadmap, and process development.

A TIME LIKE NO OTHER

SWEEPING CHANGES CHALLENGE THE INDUSTRY AND THE TECHNOLOGY



BY DAVID LAMMERS

Has there ever been a time like this, with so many technical and business challenges facing the semiconductor industry almost simultaneously? The list is daunting: industry consolidation, EUV lithography, FinFETs, through-silicon vias, 450mm wafers, and new memory types.

For this writer, a comparable period of intensity came in the mid-1980s, when the transition to CMOS coincided with Japan's investment push. U.S. companies bailed out of DRAMs and into microprocessors. Trade frictions boiled.

Ironically, Japan's manufacturing excellence helped it dominate then, while Japanese companies are now figuring out how to adapt and survive in a gigafab era. Three decades ago, PCs drove demand, while growth in the current era is driven by smartphones and tablets, products that didn't even exist in the mid-1980s.

The myriad technical and business challenges facing the semiconductor industry make this a time unlike any other, according to analyst Bill McClean, president of IC Insights.

"Most people in the industry just don't realize how fast things are changing," McClean said. Throughout most of its history, there were a dozen or more companies which invested heavily, including half a dozen Japan-based companies. Now, investments have concentrated largely in just a few top players, while the so-called second-tier companies have sharply moderated their fab spending plans.

Spurred by competition from GLOBALFOUNDRIES and Samsung, and calls for more capacity from its top customers, TSMC has roughly doubled its capex spending in recent years, McClean said, shaking his head in wonder at the company's change in spending behavior. IC Insights recently reported that the top three spenders for 2012—Samsung ($13.1 billion); Intel ($11.2 billion); and TSMC ($8.3 billion) will account for slightly more than half of the expected $61.4 billion in semiconductor capital expenditures forecast for 2012. If SK Hynix ($3.7 billion); and GLOBALFOUNDRIES ($3.1 billion) are added to the mix, the five largest spenders will account for 64% of the total, according to IC Insights (see figure 1).

Chris Moran, vice president of strategy at Applied Materials, said the industry may have faced a similar mountain of challenges during the transition to 300mm wafers and copper interconnects. "We've had these big technical changes

Chris Moran, vice president of strategy at Applied Materials

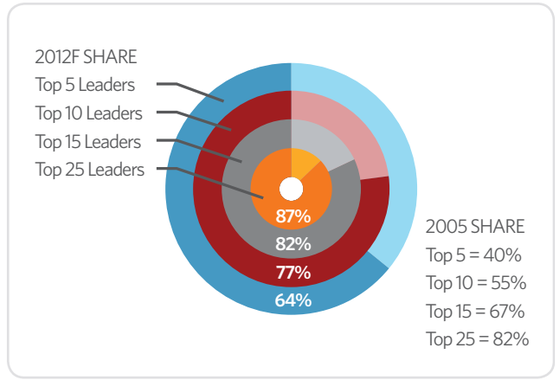


Figure 1. 2012F Capital spending leaders' shares of total worldwide semiconductor industry spending ($61.4B). Data source: IC Insights

before. What is striking now is that there are a lot fewer customers. As consumers, we may all benefit from the higher efficiencies created by the technology and scale of these large companies, but the equipment industry must develop sustainable ways to deal with ever-increasing technology and business complexities," he said.

Lithography expert Chris Mack sums it up: "Only the biggest players will survive, and the survivors will get bigger."

ADDING PROCESS COMPLEXITY

However, the greater complexity of these new technical challenges also makes them expensive. In order to maintain performance and reduce power consumption,

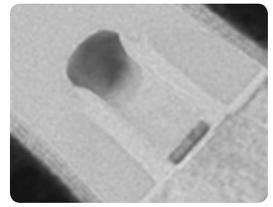


Figure 2. TEM of a 32nm gate-first HKMG device. Image courtesy of GLOBALFOUNDRIES

semiconductor companies have become more creative, coming up with techniques such as strained silicon, replacement gate high-k, and immersion lithography.

Strained silicon, for example, requires new epitaxial deposition steps, and high-k/metal gate technology (see figure 2) serves to reduce gate leakage while adding atomic layer deposition (ALD). The drive to 20nm and 14nm will add

A TIME LIKE NO OTHER

SWEEPING CHANGES CHALLENGE THE INDUSTRY AND THE TECHNOLOGY

double patterning and additional etch steps, while high-mobility germanium and indium gallium arsenide channels (see figure 3) will require more epitaxial deposition. That will boost demand for more process tools, as chip makers redouble efforts to control process costs.

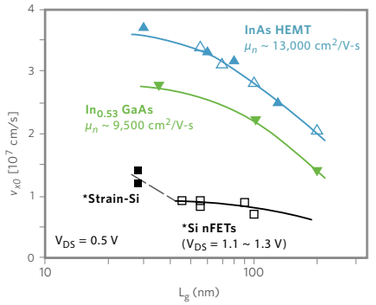


Figure 3. III-V improves performance at V_{dd}=0.5V vs. Si. Data source: SEMATECH

EUV CHALLENGES

Much less predictable than the industry consolidation trend is how the technical challenges will play out, with the biggest question mark hanging over the commercial viability of EUV lithography. If EUV throughputs lag, patterning will be so expensive that companies may slow down the cadence of Moore's Law scaling, said imec CEO Luc Van den hove. Already, companies plan to introduce a first-generation 14nm node with double patterning lithography that will not achieve the expected SRAM density doubling. Later, if and when EUV becomes cost-effective for the critical mask layers, those companies will jump to a second-generation 14nm technology with true density doubling, Van den hove said.

EUV's success is so critical that ASML, which has an effective monopoly in the EUV field, was able to convince its top customers to share the cost of next-generation EUV and 450mm lithography development, selling shares to Intel, Samsung, and TSMC, with Intel's investment potentially reaching the $4 billion plus level.

Further, ASML's planned acquisition of Cymer, a supplier of EUV light sources, underscores the need to reduce risk and accelerate the introduction of this complex technology.

EUV source power, which directly impacts the wafer per hour (wph) throughput of EUV scanners, is only one of the major challenges facing EUV. Hans Meiling, director of EUV product management at ASML Holding NV, said throughputs need to be at 70 wafers per hour next year, with source power increasing to "full power" (200–250 Watts) by 2014 to reach 125–150 wafers per hour.

And the bar keeps getting higher for EUV. At the 2012 International Symposium on Extreme Ultraviolet Lithography, held in Brussels in early October, the 25-member steering committee issued a surprising call for 500–1,000 Watts by 2016. Kurt Ronse, chair of the symposium and director of lithography at imec, said the higher targets relate to the expected sensitivities of EUV resists, particularly for the contact holes, which are exposed with slower photoresists, requiring more photons and thus, more source power.

The pressure is similarly high for creating an EUV mask infrastructure. Stefan Wurm, a GLOBALFOUNDRIES assignee to Sematech who runs the Consortium's lithography program, said he is less worried about source power now than the challenges of getting defect-free EUV mask blanks and patterned reticles. Franklin Kalk, CTO at Toppan Photomasks, agreed, saying that the industry needs "zero defects in the 10–15nm range by the 10nm node. That will be tough, because today we can't find all of the defects which print. EUV brings with it huge metrology challenges."

JAPAN INVESTMENT REBOUND

How will Japan-based companies cope with the trend to bigger leading-edge fabs, equipped at some point with 450mm tools and expensive EUV scanners?

Toru Watanabe, president of Applied Materials Japan, said Japan continues to supply many of the critical materials—ranging from wafers to photoresists—and will remain a leader in that area. And several of the world's top equipment vendors are based in Japan, though they, like other suppliers in the U.S. and Europe, face challenges from lower cost vendors emerging in Taiwan and South Korea.

Toru Watanabe, president of Applied Materials Japan

Japan-based semiconductor companies are in the process of sharpening their focus on specific product areas, going from companies that "tried to cover all areas." Sony, for example, has become the dominant supplier of CMOS image sensors for Nikon and other leading digital camera makers. And Toshiba will continue to invest in leading-edge tools for NAND flash.

This year and next will prove to be an important transition period for Japan's semiconductor industry, Watanabe said. "A lot of big things happened this year. Renesas said it will shut down almost half of its fabs, and others will shut down manufacturing as well. Next year will be a restart and recovery time. There was not much investment in Japan this year because of the restructuring. Next year, we believe we are going to see a restart in investment."

JAPAN'S FUTURE

Bill McClean said several of Japan's semiconductor vendors are "adjusting their business models, carving out their niches" in automotive ICs, NAND flash, mobile DRAMs, and the like. Other companies, such as Fujitsu, are deciding how they might exit the chip business and concentrate on their core systems businesses.

Seven years ago, according to IC Insights, Japan-based companies accounted for 22% of worldwide capital investments. This year, Japan is on track to invest about 9% of the total (see figure 4), and McClean said he sees several of Japan's chipmakers continuing "a defensive posture."

Toshiba, along with its NAND flash partner SanDisk, will build a 450mm fab at some point, as they continue to, as McClean put it, "put their stake in the ground as a leading-edge vendor."

However, the yen-dollar exchange rate puts Japan-based manufacturers in a tough position. With the yen trading at about 80 yen to the dollar, McClean said "it is tough for Japanese companies to compete" in cost-sensitive consumer areas.

Joanne Itow, foundry analyst at Semico Research, said Japanese companies have opportunities as the world shifts to new energy paradigms. Combining sensors and micro-controllers, for example, could be used to reduce energy consumption. The "Internet of Things," with home appliances linked to the Web, is another opportunity.

Japan needs to encourage an entrepreneurial culture, Itow said, and not rely on the "old conglomerates."

"I think they are picking the right areas to focus on for development," she said.

Asked about the mood in Japan, Watanabe said he sees an improving atmosphere compared with the first half of 2012. "Remember that earlier this year Sharp stopped some of its display manufacturing, and Renesas said it would close several of its older fabs. Panasonic and Sony had huge losses in their TV businesses. So it is quite natural that people became somewhat pessimistic."

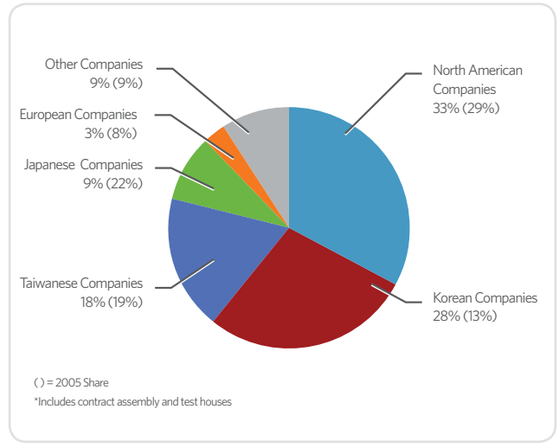


Figure 4. 2012F and 2005 share of capital spending. Data source: IC Insights

A TIME
LIKE NO OTHER

SWEEPING CHANGES CHALLENGE THE INDUSTRY AND THE TECHNOLOGY

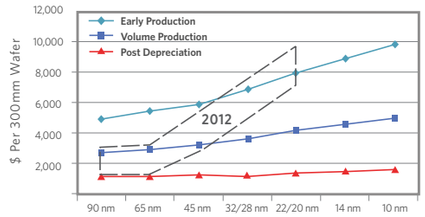


Figure 6. Manufacturing cost for different nodes at three stages of production. Data source: Gartner

However, even after these public announcements, the companies continued manufacturing and the impact was less than expected. Then Elpida announced its merger with Micron, and the Japanese government and private equity firms said they may invest in Renesas. Demand for power ICs has remained strong, often in 200mm fabs, and Japan's continued strength in automobile production supports demand from Japan-based IC suppliers.

"Supply and demand came into better balance than in the early half of the year, and we are ready to do more business next year," Watanabe said. The bigger challenge is that in the face of the high valuation of the yen, electrical generation problems, and other issues, many Japanese people "have become rather negative. Business was crazy good until 1992, but for 20 years the economy has not been so good, even as other Asian countries keep getting better and better."

"All of the Japanese people are trying to figure out what Japan should be like in the next 10 or 20 years. What everyone agrees on is that Japan needs to change."

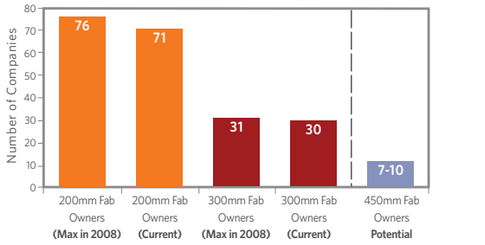


Figure 5. Number of companies with 200mm vs. 300mm fabs. Data source: IC Insights' Strategic Reviews Online database

EXPENSIVE 450MM TRANSITION

One worrisome topic, still under debate, is whether the semiconductor industry can continue to deliver on the 30% per annum reduction in the cost per function at the heart of the chip industry's success. If it costs more to make tomorrow's transistors, with EUV and process complexity as the leading causes, will revenue growth continue its upward trend?

The largest semiconductor companies have turned to the 450mm wafer transition as one answer to wafer processing costs, environmental impacts, and fab throughputs. However, Moran said the view at Applied Materials is that only a few companies—five or six at the most—will ever build 450mm fabs (see figure 5). Once the transition to 450mm production for high-volume products is completed, one $10 billion fab may be able to produce $30–40 billion worth of ICs, equivalent to a tenth of today's semiconductor industry production.

For the midterm, other companies will stay on 300mm wafers but push transistor scaling (see figure 6). "Equipment companies will have to develop two more nodes of leading-edge 300mm tools, even after 450mm manufacturing gets started. That will be wildly expensive and the industry will have to investigate more productive R&D methods to keep our cost in line with the opportunities," Moran said.

That attitude—that somehow the semiconductor industry will figure it out, dealing with its challenges as it always has managed to do—seems to prevail. "Forty years of scaling have shown that, ultimately, people find a way," Moran said.

Veteran journalist David Lammers, formerly Tokyo Bureau Chief for Electronic Engineering Times, has covered the semiconductor industry since 1985.

MACOM Technology Solutions

FABULOUS TOOLS

OLD BUT FAITHFUL:
ALWAYS THERE WHEN YOU NEED IT

It's a fair bet that after more than 40 years in business, Applied Materials has semiconductor production tools installed in virtually every fab in the world. So at any moment of any day, somewhere on the planet someone is building semiconductors on an Applied Materials system. This got us wondering about whatever happened to all those tools we sold years ago.

Got a FABulous story about a production tool legend? Share it with us at nanochip_editor@amat.com.

When Thomas C. Parolisi, presently equipment service group leader at M/A-COM Technology Solutions Inc. ("M/A-COM Tech") in Lowell, Massachusetts joined M/A-COM, Inc. in 1989, little did he know he was about to begin a relationship with a Varian medium-current ion implanter that would continue to this day. In fact, that machine—serial number 1 (S/N 1), the first of 842 E220 EHP ion implanters that were ultimately manufactured—recently celebrated its 25th anniversary.

M/A-COM Tech is a leading supplier of high-performance analog semiconductor solutions for use in radio frequency (RF), microwave, and millimeter wave applications. Its Lowell facility fabricates gallium arsenide (GaAs) and silicon-based components.

Parolisi recalls that his first assignment was to assist in moving the tool and other equipment from its original owner, Adams-Russell Electronics, to M/A-COM Tech. Prior to the move, Parolisi had to run the tool for 24 hours straight to build up an inventory of wafers because it wasn't going to be installed immediately—installation costs were high at the time and there wasn't yet a clean room for it. As he remembers, the tool was finally installed in the summer of 1991 after the company found it was unable to get reliable product from off-site vendors doing the implant.

Many upgrades have been installed on S/N 1 over the years, as might be expected with a tool of this vintage, "It has most of the bells and whistles of any new tool out there and we consider it state-of-the-art," said Parolisi. "The reason we don't replace it? It does the job just fine." The tool is also unique in that there isn't another tool of the same vintage in the entire fab. "For a tool to still be running in good operating condition after all these years is pretty amazing," said Parolisi.

M/A-COM Tech actually has a second E220 system, S/N 374, which is used only for silicon. S/N 1 is used exclusively for GaAs, and Parolisi noted that although S/N 1 has no backside coolant function, it isn't desired anyway in this application because gallium is very fragile.

From time to time the company has considered eliminating one of the tools—the fab has proven it could run both GaAs and silicon processes on the same tool. S/N 374 is run at high dosing levels, and therefore more maintenance is required, so a motivation for replacing the older medium-current S/N 1 with a higher-current model would be that a higher-current implanter would reduce maintenance requirements and also would lead to lower operational costs, because one tool could conceivably run both GaAs and silicon processes. However, Parolisi said, "We prefer not to put all our eggs into one basket," and so S/N 1 is still in use.

The E220 was the precursor to the E500, a higher-energy version designed to meet new requirements for emerging process requirements. The single-wafer platform of the "E-Series" medium-current tools led to the single-wafer VIISta platform, which all four of Varian's semiconductor products—medium current, high current, high energy and ultra-high dose—currently utilize. There is an active installed base of 729 E220 models in the field, which Applied continues to support with parts and services.

"The tool has never been a limiting factor in what we could get out of the fab," said Parolisi. "It's kind of like Old Faithful—it's always there when you need it."

Thanks to Debra Vogler, president of Instant Insight, Inc., for support of this story.

SPOTLIGHT ON ITRS ROADMAP

ITRS FACTORY INTEGRATION UPDATES AIM TO BOOST FAB EFFICIENCY

BY JAMES MOYNE

The International Technology Roadmap for Semiconductors (ITRS) is probably the single most important document governing the direction of the semiconductor manufacturing industry. The roadmap's guiding principle is to keep the industry on pace with Moore's Law by maintaining the decades-long trend of 30% per year reduction in cost per function.

The roadmap sets targets for future manufacturing capabilities, identifies areas where technologies don't exist to meet specific capabilities, and highlights emerging technologies that could be harnessed to meet them.

The roadmap is divided into chapters representing the various aspects of semiconductor manufacturing. The factory integration (FI) chapter focuses on enterprise systems that are designed and integrated for efficient, effective development and manufacturing. Semiconductor FI experts from around the world make up an FI Technology Working Group (TWG) to evaluate the challenges, determine near- and longer term technology requirements, and set forth potential solutions.

The FI TWG is currently organized into five teams. Each team is concerned with one of the following:

1. Factory operations
2. Production equipment
3. Automated material handling systems
4. Factory information & control systems
5. Facilities

The entire ITRS is updated every odd year. Major revisions made during 2011 were published in 2012. The 2011 FutureFab publication summarizes the events of the 2011 major ITRS revision year.[1,2] Because only minor revisions were made in 2012, this article will summarize the 2011-12 chapter structure and provide a glimpse into plans for 2013.[3]

FI ACTIVITY FOCUS 2011-12

The chapter's factory integration requirements drivers are summarized in figure 1.

The chapter breaks up the list of FI difficult challenges into shorter term (through 2019) and longer term sections, as follows.

FI difficult challenges through 2019

1. Responding to rapidly changing, complex business requirements
2. Managing ever-increasing factory complexity
3. Achieving growth targets while margins are declining
4. Meeting factory and equipment reliability, capability, and productivity requirements per the roadmap
5. Emerging factory paradigm and next wafer size change

Cycle Time Reduction & Operational Flexibility	➡	**Cycle Time Operational Flexibility:** Multiple lots per carrier and/or fewer wafers per carrier. Get new products to customer much faster.
More Good Wafers Out Per Tool	➡	**Ouput Per Tool Must Increase:** Find breakthrough solutions that result in significant increases in good wafer out and increased OEE (eg: APC, e-Diag)
Highly Automated Factory	➡	The 300mm factory is much more **automated** and must be designed to transport hot-lots and hand-carry's.
Reduce Time to Money	➡	**Reduce Time to $$$/Cycle-time reduction:** What are stretch goals for cycle time from ground-breaking to first full loop wafer out. How to achieve quicker shrink?
Factory Size Is Becoming An Issue	➡	**Increased Floor Space Effectiveness:** Don't want each new generation to drive big increase in cleanroom size, especially since fab is segregated Cu/non-Cu and new metal layers added at each node.

Figure 1. ITRS factory integration requirements drivers.

FI difficult challenges beyond 2019

1. Meeting the flexibility, extendibility, and scalability needs of a cost-effective, leading-edge factory
2. Managing ever-increasing factory complexity
3. Increasing global restrictions on environmental issues
4. Post-conventional CMOS manufacturing uncertainty

Some issues cited as making these challenges difficult include:

- **Integration of fab and facility management control**
- **Lack of and the need for increased emphasis on communication standards**
- **Maintaining availability and productivity**
- **Supporting the move from reactive to predictive systems**

FI potential solutions to address these challenges, meanwhile, are presented both through narrative and via tables that define the relevant technologies. A timetable also is given for the migration of these technologies from research through development, qualification and pre-production, and ultimately continuous improvement.

Some potential solutions cited in the latest roadmap include:

- **Designed-in APC inside or outside the tool, communicating with a fabwide system**
- **Fingerprinting and equipment health monitoring**
- **Enhancement of equipment systems to support move from reactive to predictive**
- **A common prognostics and health management (PHM) capability across tools**
- **Standardized equipment data model**
- **Built-in chamber matching: movement from chamber variance reporting to chamber variance correction**

A review of the 2011-12 FI chapter shows that FI TWG efforts are strongly focused on topics such as moving from reactive to predictive, integration (for example, fab and facilities), and mechanisms for improved control and repeatability.

The 2012 ITRS roadmap provides a complete presentation of the challenges, issues, and potential solution roadmap for FI in semiconductor manufacturing. To download the roadmap, visit http://www.itrs.net and follow the appropriate links.

SPOTLIGHT ON ITRS ROADMAP

ITRS FACTORY INTEGRATION UPDATES AIM TO BOOST FAB EFFICIENCY

LOOKING AHEAD TO 2013

As we move into the 2013 major revision year, a number of changes to the FI chapter and even to the FI TWG are being considered. Here is a summary.

Eliminate the "Silo-ing" of Specifications

As mentioned, the FI chapter is broken into subchapters (figure 2), each with its own set of roadmap specifications. This approach was appropriate for the 1990s and 2000s, but the information age has forced a reevaluation.

For 2013 it has been proposed that these "silos" be eliminated, and information technology be presented as common to all areas. This will highlight technological commonalities across the fab and facilities, and even up-and-down the supply chain. It will promote a stronger level of integration and standardization, and also will allow for consistent incorporation of non-nanomanufacturing FI technologies into the roadmap.

The net result of this fundamental change to the FI chapter is that subchapters will likely be reorganized or eliminated, probably along data-driven boundaries rather than physical partitions.

New Challenges and Potential Solutions

2013 updates likely will focus on continued emphasis of some of the 2011-12 concepts, but will also introduce new challenges and potential solutions.

- **FI solutions for 300mm and 450mm.** FI requirements and solutions for 300mm and 450mm should be fundamentally the same to allow for leveraging of technologies across these domains and promote smooth FI migration from 300mm to 450mm technologies.
- **Looking outside the semiconductor industry.** Considering the acceleration of information technology in recent years, FI more than any other ITRS chapter must consider solutions from other industries. Challenges such as moving from reactive to predictive, big data, and supply chain integration are pervasive across all of manufacturing. The semiconductor industry must accelerate its adoption of general manufacturing solutions.
- **A more data-driven approach.** The advent of concepts such as cloud computing and autonomous agents is part of a larger movement toward data-driven solutions. The FI chapter may be reorganized to promote commonality of data-driven solutions across all elements of the FI space.
- **Addressing the big data problem.** The amount of data available today delivers benefits but also creates challenges in dealing with data sizes and rates. These challenges aren't unique to the semiconductor industry, though, and a roadmap is needed that addresses the big data problem while also aligning the semiconductor industry with other manufacturing arenas.
- **An increased focus on moving from reactive to predictive.** This concept has been accelerated in the FI chapter over the past few years and will continue to grow in importance. Concepts such as predictive maintenance, predictive scheduling and metrology prediction ("virtual metrology") will be expanded to support yield prediction and fab component simulation in lock-step with reality. The roadmap will draw heavily from other industries and focus not only on prediction technologies, but also on migrating existing systems to "prediction-ready" systems.
- **Rethinking key performance indicators (KPI).** A good example is the need to define the wait time waste metrics for equipment productivity, currently a SEMI standardization effort. (SEMI is a standards body for the semiconductor manufacturing industry.)
- **New control paradigms.** Centralized control is being questioned in other industries and should be addressed in the FI roadmap. The possibility of autonomous control ("autonomous agents") should be considered, and predictive control should be explored as part of the movement from reactive to predictive. Control performance should be quantified. Time-based (i.e., time-synchronized) control should be considered in some instances.
- **A stronger focus on technology ramps and costs.** As technology cycles get shorter, the importance of technology ramp speed and cost grows. Specific challenges, solutions and metrics for technology ramp should be considered. For example, the integration of process control and design for manufacturability techniques should be considered to reduce the number of redesign cycles in a new technology ramp-up.
- **FI technologies as barriers.** The importance of FI technologies continues to grow in the fab to the point that, in some cases, these technologies might be barriers to achieving the next technology node. For example, process control (e.g., run-to-run control), once an add-on technology, is now a required technology in most 300mm processing. For some emerging technologies it's a prerequisite to achieving necessary yields. Such critical FI technologies must be identified and a roadmap for them devised, in order to keep pace with the overall ITRS technology requirements.

Figure 2: 2011-12 Factory integration subchapters organized by technical focus.

SUMMARY

The FI chapter of the ITRS focuses on integrating factory components to efficiently produce the required products in the right volumes on schedule while meeting cost targets. Over the past two years this chapter has been updated to focus on prediction, facilities integration, and other technologies that will be required components of the fab of the future.

As we move into 2013, another major revision of the FI chapter is being considered. This revision will better address FI challenges in the information age by eliminating roadmap silos and looking at common technology solutions across the FI space.

For additional information, contact james_moyne@amat.com

Acknowledgments: We are grateful to all members of the FI TWG, especially Dr. Gopal Rao, for supporting the group's work and contributing to the FI chapter content.

[1] *R. Oechsner, "ITRS Chapter: Factory Integration," FutureFab International, Issue 40, January 2012.*
[2] *www.itrs.net.*
[3] *J. Moyne, "International Technology Roadmap for Semiconductors (ITRS) Factory Integration Chapter Update: 2013 Major Revision Plans," (invited), APC Conference XXIV, Ann Arbor, Michigan, September 2012.*

ABOUT THE AUTHOR

James Moyne is the standards and technology specialist for Applied Global Services at Applied Materials, and also is an associate research scientist in the department of mechanical engineering at the University of Michigan. He has been a member of the FI TWG within the ITRS for four years and is expected to chair the FI TWG for 2013-14. For the last two years, the FI TWG has been chaired by Dr. Gopal Rao of Intel, who will remain active in the FI TWG to facilitate a smooth transition of leadership and provide invaluable technical input. Also, it is expected that Dr. Jonathan Chang from Taiwan Semiconductor Manufacturing Corporation (TSMC) will serve as co-chair, with the aim of succeeding Moyne in the leadership position in 2015.

CUT SOLAR COSTS AND INCREASE YIELD

WITH BETTER PREDICTION OF WIRE BREAKAGE

BY JIMMY ISKANDAR AND JAMES MOYNE

Silicon accounts for approximately 20% of the total cost of a multi-crystalline solar module. Manufacturers are now looking for ways to reduce this cost as much as possible. One strategy is to improve the yield of the wafering process, which depends on the wire saws that slice silicon bricks into wafers (see figure 1).[1]

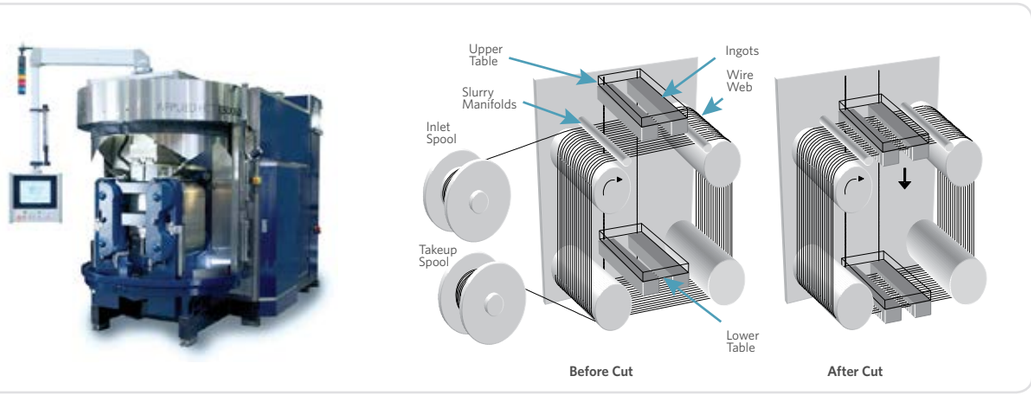


Figure 1. Wire saw system on left, cutting assembly on right.

A review of data from a solar-panel manufacturer showed that wire breakage (WB) accounts for 25% of all failures on a particular tool set. WB typically occurs multiple times per month and results in a total downtime of 1 to 2 hours per tool per month. Additionally, quality yield, a fundamental driver of total cost of ownership, is a challenge; yield levels lower than 90% were observed 32% of the time, causing 74,000 wafers lost per tool annually.

Consequently, there is strong interest in the ability to predict and prevent both WB and low-process yield.

DEVELOPING PREDICTIVE MODELS FOR WB AND YIELD

When impending breakage or poor yield is predicted during normal operation, that information can be used to plan maintenance and avoid disruptive, unplanned system stoppage and conditions that cause yield loss. This prediction capability can reduce downtime, wafer scrap, overall system disruptions and maintenance costs, thereby lowering the overall cost per good wafer out.

Predictive models are developed by leveraging automation software solutions such as Applied E3 fault detection and classification (FDC) or statistical process control (SPC) systems. Historical tool data collected via these systems is analyzed to develop multivariate prediction models that relate equipment state information to maintenance events. These models are exercised during run-time to determine if and when maintenance is needed.

The predictive model development process consists of the following steps:

1. **Collection and preparation of historical data**
   FDC and SPC statistics are collected along with tool maintenance and yield information. The data set must be of sufficient length so that a stastically significant number of WB and varying qualities of yield are observed, and must be categorized to indicate which data belongs to good or bad runs. The data also may need filtering; for example, to remove the impact of external events that might hide the prediction signal, or to remove data from immediately before breakage that might hide or "swamp" the long-term prediction signal.
2. **Data merging**
   Historical tool and maintenance data must be aligned, usually with time as a key parameter, and yield measurements merged with the tool data.
3. **Data strengthening**
   The merged data is analyzed and, wherever possible, its quality is improved using techniques such as outlier removal, data overlays, interpolation, and categorizing.
4. **Data reduction to determine important sensor statistics**
   The large data set is analyzed using a variety of multivariate techniques to determine which sensors are most important to the prediction process.
5. **Multivariate prediction model development**
   The reduced data set from step 4 is used to develop multivariate models. As part of this process, simple univariate limit models are employed to develop a multivariate limit model. In future works, more advanced techniques such as partial least square (PLS) and support vector machine (SVM) will be employed.

PREDICTING WB

In applying the predictive maintenance (PdM) process to predict WB, the goal is to predict WB hours in advance. To this end historical data was collected over 1 month from 38 tools, each with 133 sensors, and this data was merged with maintenance information. For each sensor, hourly minimum, maximum, mean, range and area statistics were calculated, and the data analyzed as described above to develop predictive models.

When WB occurs, a number of sensor stastics show large value spikes immediately before and/or after. For the purpose of meaningful prediction, this data was filtered out as part of the data-strengthening process because it is only useful for notification. The remaining data is divided into three categories: WB failure, "other" (i.e., non-WB) failure, and "good," representing normal process runs.

To determine which are the important sensor statistics, we used univariate and multivariate analysis iteratively. We selected potential sensor statistics that correlate with WB, and filtered out those with very low variation or with a high correlation to a sensor statistic we had already selected. PLS was then employed iteratively to rank the sensors and determine a reduced set. The result is a set of sensor statistics (see figure 2) that collectively provide a promising distinction between WB data and normal data.

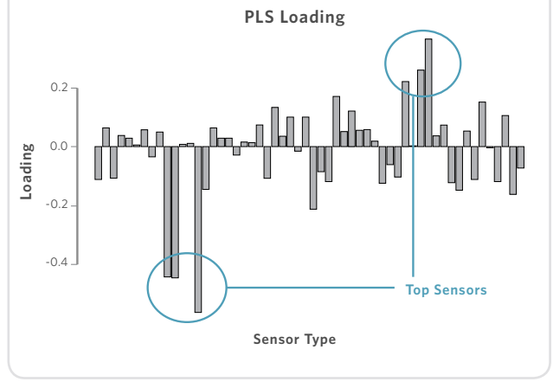


Figure 2. PLS loading, by indicating the strength of the parameter contribution, points to the top-ranked sensors contributing to the signal.

CUT SOLAR COSTS AND INCREASE YIELD

WITH BETTER PREDICTION OF WIRE BREAKAGE

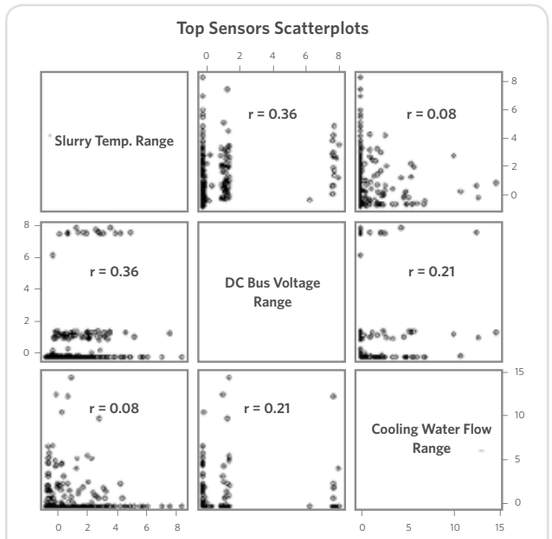


Figure 3. Illustration of low correlation among top sensor statistics.

The matrix of plots in figure 3 shows that the parameters have low correlation (the off-diagonal plots have low 'r' values, indicating little correlation between pairs of sensor statistics). This means that each of these sensor statistics brings a unique contribution to the prediction process.

We analyzed the contributions and determined that combining two sensor statistics—slurry temperature and DC bus voltage—produced a good prediction model. However, there were a number of false positives (i.e., false indications of WB). To reduce them, we suppressed any alarm that appears within a fixed time frame after a previous alarm. (The timeframe was derived from a process MTBF analysis.) The resulting combination of multivariate prediction and suppression of false alarms represents the PdM model.

Why these two particular statistics? It makes sense that these two are important to WB prediction. Slurry temperature has a major impact on slurry viscosity—a slight temperature rise causes a big viscosity drop. As a result, the wire exposes itself directly to an ingot, creating friction and potential failure. DC bus voltage is the power supply to the motor, and sharp fluctuations in it cause motor instability—again creating disruptions in the wire movement through the ingot.

PREDICTING POOR YIELD

Yield data from 162 full-load (full capacity) cuts across 17 tools were used for the yield analysis. Hourly minimum, maximum, mean, range and area statistics were calculated for the 133 sensors. The data was merged with the yield data, and categorized as low, normal, or high yield (see figure 4). This categorization provides contrast as to which sensor statistics are associated with high variation in yield.

A technique called "rules ensemble" was employed to rank sensor statistics in order of their importance in the determination of yield.[2] Three highly ranked sensor-statistics were picked for the yield-prediction process: bearing box water cooling amount area, water cooling amount area, and slurry cooling minutes. These were picked because (1) they have a high ranking in the rules ensemble data reduction process and a low correlation with each other; (2) they agree with process knowledge as determined through consultations with process experts; (3) they can be predicted with a limit model; and (4) they are easy to inspect.

It makes sense that these sensor statistics would relate to yield prediction. For example, when the rotation precision of a bearing box decreases, each cut generates more heat and more cooling water is needed for the bearing box. Therefore, the total amount of cooling water needed for one cut will increase. Slurry temperature rises after a cut and a nonoptimal cut generates more heat. Therefore, heat generation indicates a suboptimal operating condition that results in lower yield.

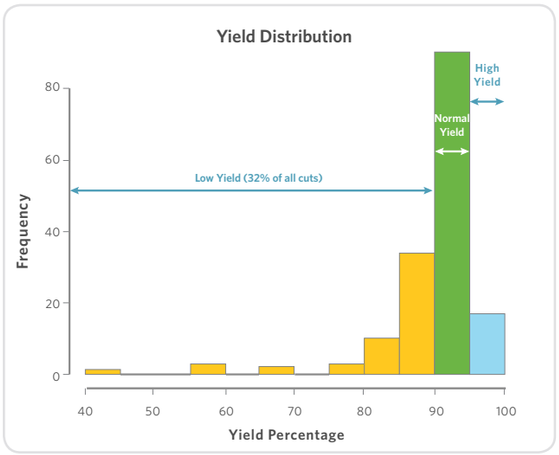


Figure 4. Quality yield histogram.

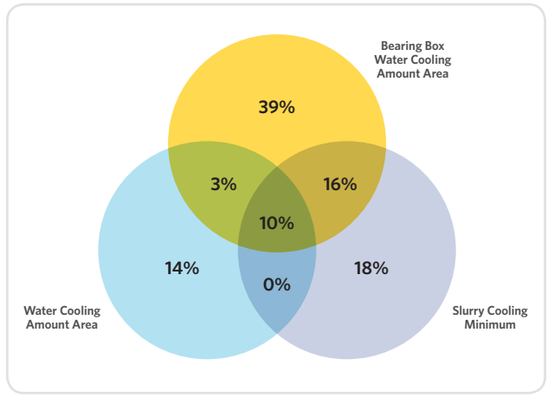


Figure 5. Quality yield prediction contribution from univariate models.

Once we identified these "high impact" sensors, we created a yield-prediction limit model for each sensor statistic. An alarm is sent when a sensor statistic is above its limit. (With successive alarms, only the first is sent because only one alarm is needed per cut.) A high number of false alarms (i.e., an alarm is sent, but the cut nevertheless results in high yield) is permissible because tool inspection can be done following the cut, and inspection of these three sensors is nonintrusive and inexpensive.

Figure 5 summarizes the contributions of the individual univariate models to overall quality yield prediction. Overlap regions show duplicate predictions between models. While there is overlap between the models, the majority of the prediction space (39%+18%+14% = 71%) can be predicted effectively with univariate models and an analysis of the remaining prediction space revealed that the univariate models did not provide conflicting predictions (i.e., one predicting bad yield and the other(s) indicating good yield). Therefore we concluded that univariate models could be used effectively in this instance. The model outputs were combined so that, in the case of multiple models generating alarms, only one alarm was reported.

RESULTS

For the PdM application, the WB prediction model could be applied to 81% of the tools. Models for the remaining 19% couldn't be developed given an unacceptably high rate of false positives. When we applied the model it predicted WB occurrences 57% of the time at a median of 40 hours in advance, with a 4% false positive rate (see figure 6). Note that this means—for these tools—over half the unscheduled downtimes and related scrap associated with WB events are eliminated. The solution also predicted other failure modes as well. The total downtime saving per month per tool is 5.9 hours, which translates into $26,000 per tool per year.

The low-yield prediction model predicts and enables prevention of impending yield loss 68% of the time (see figure 7). The result is a net savings of $41,000 per tool per year, not including improvements related to higher overall yield, lower scrap, and lower maintenance costs not quantified in this study.

CONCLUSION

Both PdM and predictive yield have great potential to impact cost of ownership in nanomanufacturing. These capabilities are an important part of Applied's prediction strategy, which will leverage our E3 automation and equipment engineering system capabilities to support customers as we move from a reactive to a predictive mode of fab operations.

For additional information, contact jimmy_iskandar@amat.com or james_moyne@amat.com

[1] *Iskandar, J., Moyne, J., Schwarm, A., and Liu, H. (2012), Predictive Maintenance of Wire Breakage and Quality Yield of Wire Saw Tools with Multivariate Limit Model, 27th European Photovoltaic Solar Energy Conference (EU PVSEC), September, 2012.*

[2] *Friedman, J. H. and Popescu, B.E. (2008). Predictive Learning via Rule Ensembles, The Annals of Applied Statistics 2008, Vol. 2, No. 3, 916–954 DOI: 10.1214/07-AOAS148, Institute of Mathematical Statistics.*

WB Prediction Rate	58%
Non-WB Failure Prediction Rate	56%
False Positive	4%
Tools Without Model	19%
Median WB Prediction Time (hours)	40
Median Non-WB Failure Prediction Time (hours)	50

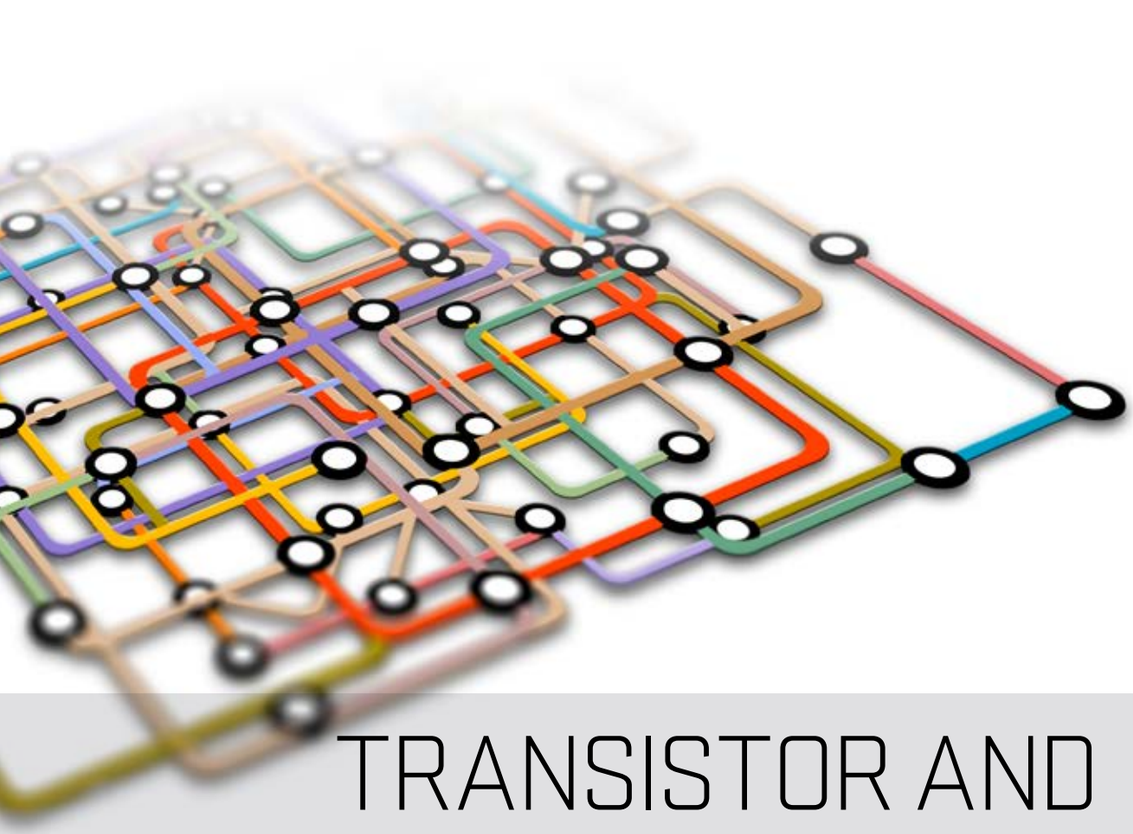
WB = wire breakage failures
Non-WB = non-wire breakage failures
Tools without model = % of tools for which wire-breakage prediction models could not be developed

Figure 6. WB prediction results.

Prediction Accuracy	68%
Tool Participation	71%
False Positive	77%
Average Saving Per Tool Per Year	$41,000

Tool participation = the number of tools participated in prediction; those which do participate are due to unacceptably large number of false positives
*Average saving per tool per year = 10% yield loss * prediction accuracy (68%) * tool participation (71%) * percent low yield (32%) * 2300000 (number of cells produced per year) * $1.15 (price per solar cell)*

Figure 7. Quality yield prediction result.



TRANSISTOR AND INTERCONNECT ADVANCES

SMOOTH THE WAY TO THE 2XNM NODE

As scaling continues to the 2xnm node, planar transistor fabrication faces growing challenges. This has prompted a transition to 3D architectures for leading-edge devices while other innovations stretch extendibility of planar scaling to the ultimate extent. Both paths forward involve greater manufacturing complexity and sophisticated engineering of materials and interfaces.

At the 2xnm node, dopant activation and defect creation in the extension, source-drain junction, and contact regions can impede scaling. Logic devices require a high-k/metal gate architecture that requires additional process steps and demands stringent process controls. Equivalent oxide thickness (EOT) scaling and gate leakage challenges drive the need for atomic layer deposition (ALD) of high-k dielectric gate stacks. For DRAM devices, new deep plasma processing is required to enable higher dose nitridation without increasing leakage current or transistor threshold voltage. High aspect ratio (HAR) etch faces the most demanding requirements to date for critical dimension (CD) uniformity and profile control in addition to new specifications for 3D structures.

Scaling is also challenging interconnect technologies. Dielectrics are becoming more porous in pursuit of lower κ values, yet must withstand stresses from extensive downstream processing and advanced packaging steps. Feature size is such that ionized physical vapor deposition (PVD) cannot guarantee the required coverage and void-free metal gap filling for electroplating.

Fortunately, advances in transistor- and interconnect-related technologies for 2xnm and beyond are proving successful in overcoming the above challenges.

TRANSISTOR CHALLENGES AND ADVANCES

Cryogenic Ion Implantation

At advanced nodes, ultra-shallow junction formation in the source/drain extension (SDE) requires extremely abrupt profiles, aided by the elimination of energy contamination in the implanted profiles as well as means to suppress diffusion. Beneficial strain incorporated to independently optimize performance of n- and p-type devices is subject to relaxation from implant misfit and threading dislocation propagation after high-temperature dopant-activation annealing.[1,2] Defects, which commonly form at the implant boundary during annealing, can become nucleation sites for dislocation formation or aid in the inter-diffusion of boron and germanium that, in turn, can accelerate this detrimental strain relaxation. Contact areas become so small that contact resistance can severely inhibit device performance, challenging integration and process engineers to increase dopant activation without incurring major process changes.

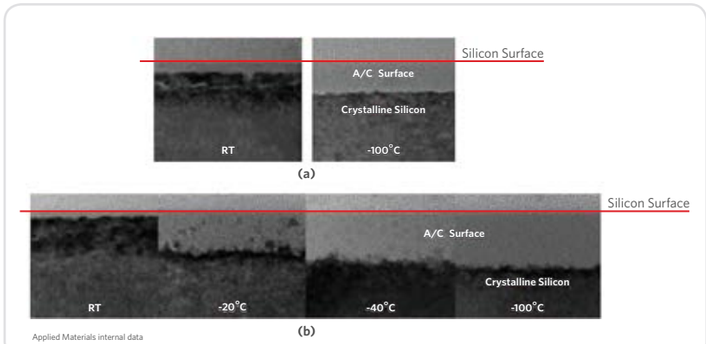
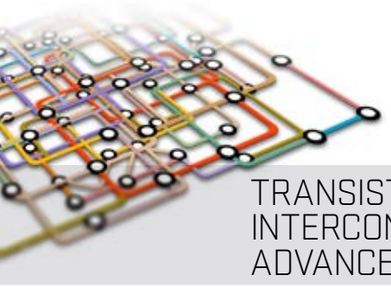


Figure 1. Cross-sectional TEM images for (a) boron 2keV 3e15/cm² at RT and -100°C; (b) carbon 5keV 1e15/cm² at RT, -20°C, -40°C, and -100°C reveal thicker amorphous layers and smoother a/c interfaces with cryo-implantation. The effect is more evident as temperature decreases.

Ion implantation has evolved on several fronts to address these issues. In particular, cryo-implantation (at temperatures as low as –100˚C) combined with energy-pure dopant profiles and special species, such as carbon and germanium, is proving versatile and effective in creating ultra-shallow junctions with minimal damage, improved activation, and reduced leakage. Cooling the wafer to cryogenic temperatures during implant promotes amorphization at lower doses and to greater depth with fewer target interstitials left beyond the amorphous/crystalline interface.[3] (See figure 1.) Fewer defects formed upon annealing greatly reduce dopant diffusion and deactivation. In addition, defect reduction preserves strain and minimizes potential junction leakage pathways.

Shallower junctions and smaller gate pitch require balancing needs for a deeper SDE to lower resistance and a shallower SDE to improve short channel effect performance. Conventional nMOS contacts have been made using arsenic ion implants, but smaller contact areas at advanced nodes dictate greater active dopant abruptness and higher concentrations to reduce series resistance. Phosphorus is an attractive alternative to arsenic; co-implantation with carbon at –100˚C overcomes the limitations of pure phosphorus implantation and enables very abrupt, low-resistance junctions.

Cryo-implantation improves nickel silicidation interface qualities, reducing the roughness that results when pFET channel stress-enhancing germanium concentrations exceed 25%.[4] Cryo-implantation also makes it possible to meet pMOS depth and abruptness requirements by trapping interstitials and limiting nickel diffusivity.



TRANSISTOR AND INTERCONNECT ADVANCES

SMOOTH THE WAY TO THE 2XNM NODE

Dielectric Gap Filling

Chemical vapor deposition (CVD) has historically enabled void-free filling of pure, dense oxides for metal isolation with minimal leakage and no parasitic capacitance. With continued scaling, though, conventional interlayer dielectric (ILD) CVD faces severe challenges of smaller features, higher aspect ratios, re-entrant profiles, and reduced tolerance for thermal and oxidative treatments.

Flowable CVD technology overcomes these challenges, enabling profile-insensitive, void-free gap filling of reentrant gaps with diameters less than 7nm and aspect ratios exceeding 50:1. The process involves the reaction of a carbon-free silicon precursor and inorganic reactant gas that produces condensation of a low-viscosity film upon the wafer substrate. The film flows to the bottom of gaps, producing true bottom-up filling. Carbon-free chemistry creates high-density, non-porous silicon dioxide comparable with industry-standard HDP-CVD silicon dioxide and ensures the absence of fixed charge.

The low thermal budget (<150˚C) process sequence also gives flowable CVD the compelling advantage of liner-free integration compatibility with tungsten and titanium nitride metal films used as electrodes, contacts, and conductive lines. These films are prone to oxidation during low-temperature steam annealing. For electrodes and narrow conductive lines, such as buried bit and word lines in advanced DRAM, the resulting resistance change can jeopardize device function. Consequently, depositing flowable CVD oxide directly on metal without a nitride liner reduces integration complexity, allows implementation of novel device architectures, and offers a means to scale devices to narrower pitch.

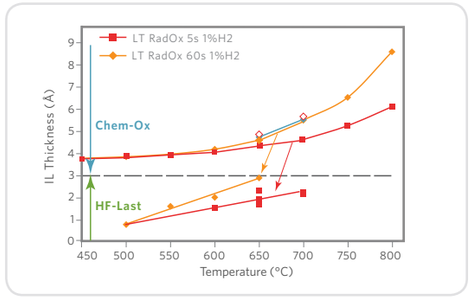


Figure 2. Radical oxidation enables controlled, repeatable IL scaling to 2Å for both gate-first and gate-last (shown above) processes.

ALD High-κ Dielectrics

Although ALD high-κ dielectrics relieved the EOT scaling roadblock when SiON reached its limit,[5] extending Moore's Law to 2xnm and beyond now challenges high-κ logic gate stack scaling. Fortunately, proven solutions are available. The oxide interface layer (IL) has a low κ value; therefore, reducing its thickness will produce a large effect on overall EOT. Both rapid thermal oxidation and radical oxidation processes offer a means to scale the IL below 8Å,[6] while scaling to 2Å can be achieved with radical oxidation (N_2O/H_2) in a controlled and repeatable fashion with a thermal budget compatible with either gate-first or gate-last sequences (figure 2). The κ-value of the ALD HfO_2 layer can be increased through post-deposition plasma nitridation and annealing, reducing the EOT by a further 1-2Å.

For ultra-thin to zero IL formation (beyond 2xnm), integrating dry plasma gate pre-clean on the same mainframe delivers the stringent IL control attainable with short, consistent, vacuum-controlled queue time between each process step. The necessary increase in the κ-value of bulk HfO_2 is achievable by incorporating a κ-boosting element, such as titanium, into the matrix during deposition.

For DRAM, scaling the peripheral gate is essential for advanced high-performance, low-power devices but current nitridation processes are limited in achieving the optimal leakage and threshold voltage. A high-temperature, high-power NH_3 nitridation process with pulsed RF plasma resolves this issue by generating the higher nitrogen doses needed for the 2xnm node without degrading leakage and threshold voltage. High power compensates for the lower nitridation rates associated with NH_3 plasma. Pulsing delivers a "soft" plasma at higher RF power and temperature. Combining these conditions with an integrated post-nitridation annealing on a common platform delivers superior nitridation. Furthermore, a unique feature of the NH_3 chemistry is the formation of NH radicals in the plasma, which is typically associated with greater process conformality. As device structures transition to 3D, this property may facilitate new nitridation applications using NH_3 plasma.

HAR Etch

Emerging 3D architectures are intensifying demands placed on etch processes, including very high aspect ratio (>50:1) etch requirements, high throughput, and very high tungsten selectivity in the case of 3D NAND staircase contacts (figure 3). The advent of 3D NAND has also increased the aspect ratio of mask etching and requirements governing mask etch rate, selectivity, and deformation.

The common element among 3D architectures is a stackable device structure comprising multiple alternating dielectric layers that exacerbate aspect-ratio-dependent etch (ARDE), a fundamental challenge for very high aspect ratio etch. The two key approaches are an oxide-poly alternating stack and an oxide-nitride alternating stack with wet etch removal of the nitride for tungsten filling.

Critical dimension uniformity and vertical profiles are especially critical (i.e., high bottom-to-top CD ratio, absence of bowing or bending, and distortion-free bottom holes). In addition, for the staircase contact, it is essential to avoid punch-through of the gate tungsten. In other words, the tungsten layer at the top of the staircase will experience more than 300% over-etching, effectively increasing the selectivity requirement to >350:1.

A new triple-frequency capacitive-coupled etch system addresses these aggressive etch performance requirements using a unique very high frequency source, optimizing RF delivery, and innovatively coupling different bias frequencies. The source enables high etch rates and throughput in hard mask etching, and high plasma density and polymerization for the dielectric etch process.

Innovatively coupling high and low bias frequencies achieves the required dielectric etch rate, profile, and uniformity. High frequency bias improves plasma density and ion energy control to optimize ARDE. Step-to-step wafer temperature control facilitates precise polymer management to simultaneously achieve very high aspect ratio etching and very high tungsten selectivity. This "active" temperature control avoids the temperature creep with plasma thermal load that would severely limit conventional wafer cooling systems in managing the multi-aspect ratio staircase etch. Wafer temperature tuning also allows for controlling sidewall passivation during mask etch, thus enabling in situ all-in-one etching of both mask and dielectric stacks.

INTERCONNECT CHALLENGES AND ADVANCES

Low-κ Dielectrics

As geometries shrink, the ability to increase device signal speed is significantly affected by the dielectric constant (κ) of the insulating materials between the copper interconnects. For ideal electrical performance, the effective κ-value (κ_{eff}) of the inter-level dielectric (ILD) and associated barrier films must scale correspondingly. In addition, advanced packaging techniques and the trend toward lead-free solder make chip packaging interaction increasingly important for high yields. Lead-free solder materials exert greater stresses on the packaged chip and in the interconnect.[7,8] Achieving κ ~2.2 for scaling to 2xnm and below necessitates re-engineering the dielectric's composition and structure to withstand downstream process steps while retaining essential mechanical properties. It also requires treatment of the dielectric following these other processes to preserve desired chemical, electrical, and mechanical attributes.

New chemistry enables the necessary material re-engineering, enhancing the mechanical strength contributed by the carbon backbone structure in contrast to the weakening effect typical of methyl in existing organosilane chemistries. As with earlier low-κ films, the engineered, nano-porous ILD is cured with ultraviolet light to drive out the labile species and set the desired mechanical strength (elastic modulus and hardness). As an added benefit, the new chemistry results in a significantly thinner transition layer between the barrier and bulk low-k film that lowers overall κ_{eff}, enhances adhesion, and strengthens the interface.

Plasma etching, photoresist ashing, wet cleaning, chemical mechanical planarization, and copper oxide removal prior to barrier deposition can disrupt the chemical structure at the surface of low-κ film.[9,10] This, in turn, can adversely affect the final κ_{eff} of the device such that the benefit of lower-κ materials is not fully realized. At 2xnm and beyond, preserving the bulk dielectric constant is essential for reducing cross-talk noise and RC delay.

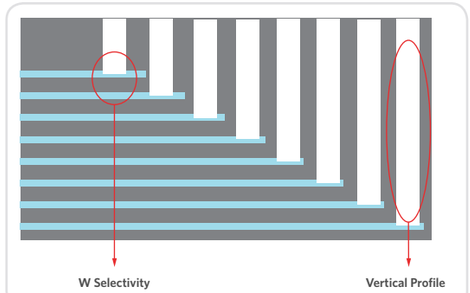
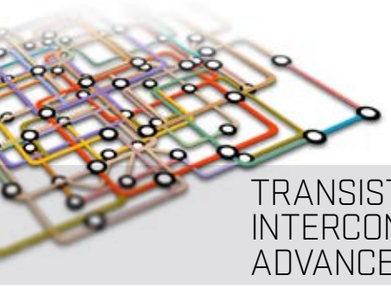


Figure 3. Critical 3D NAND staircase etch.

A novel κ-treatment process restores the desired chemical bonds. Introducing a carbon-containing reactant in the presence of an energy source creates an active supply of the methyl group for restoring the disrupted Si-CH_3 bonds and accelerates the treatment cycle. The energy treats both the surface of the film and several monolayers of the dielectric, which promotes bulk film robustness. The ILD thus retains its chemical properties without weakening its dielectric performance and the key structural properties of modulus and hardness.

Copper Barrier/Seed

Incremental enhancements of both barrier/seed and electroplating processes have enabled void-free copper gapfill as far as the 2xnm node. Beyond this, however, ionized PVD cannot ensure that barrier/seed layers achieve the requisite coverage for electroplating, making void-free gap filling extremely challenging. Even the most optimized barrier/seed process, showing conformal coverage without



TRANSISTOR AND INTERCONNECT ADVANCES

SMOOTH THE WAY TO THE 2XNM NODE

any overhang, increases feature aspect ratios beyond levels manageable for electroplating (figure 4a).

However, augmenting deposition with subsequent thermal reflow offers a potentially limitless solution to this challenge. Creating a selective profile (thinner field coverage and thicker bottom coverage) in the deposition step and then heating the wafer promotes the optimal interaction of grain boundary movement, capillary forces, and wetting properties of the underlying layer to produce bottom-up fill.[11-13]

Although temperature regimes vary with different underlying materials, lower temperatures (50-200˚C) enhance surface diffusion of copper along feature sidewalls for a moderate increase in bottom coverage; higher temperatures (~250-350˚C) enable mass movement from the field and sidewalls into the feature to effect a substantial increase in bottom coverage. The deposition, reflow, and cool-down cycle can be iterated to gradually increase bottom coverage to the point of complete fill (figure 4b). Independent temperature control for deposition and reflow steps enable the process to be used with cobalt and ruthenium liners.

OUTLOOK FOR THE 2XNM NODE

Transistor technology is advancing in multiple directions. While material properties and physical barriers are driving the growing trend from planar to 3D designs at the 2xnm node, much is being done to extend planar scaling and capability to the utmost. Anticipating these challenges, processes and systems are proving successful in enabling both approaches.

[1] *F.T. Sanuki, et al., "Sophisticated Methodology of Dummy Pattern Generation for Suppressing Dislocation Induced Contact Misalignment on Flash Lamp Annealed eSiGe Wafer," VLSI Tech., pp. 156-157, 2009.*

[2] *M. Yu, et al., "Relaxation-Free Strained SiGe with Super Anneal for 32nm High Performance PMOS and Beyond," IEDM Tech. Digest, pp. 1-4, 2006.*

[3] *Morehead, et al., "Formation of Amorphous Silicon by Ion Bombardment as a Function of Ion, Temperature, and Dose," Journal of Applied Physics, 43, 1112, 1972.*

[4] *A. Renau, "Device Performance and Yield—A New Focus for Ion Implantation," 10th International Workshop on Junction Technology, IEEE, pp. 1-6, 2010.*

[5] *K. Mistry, et al., "A 45nm Logic Technology with High-κ + Metal Gate Transistors, Strained Silicon, 9 Cu Interconnect Layers, 193nm Dry Patterning, and 100% Pb-Free Packaging," Proceedings of the IEDM, pp. 247-250, 2007.*

[6] *M.J. Bevan, et al., "Ultra-Thin SiO^2 Interface Layer Growth, "Proceedings of the 18th Conference on Advanced Thermal Processing of Semiconductors – RTP 2010.*

[7] *C. Odegard, et al., "Dielectric Integrity Test for Flip-Chip Devices with Cu/Low-κ Interconnects," Proceedings of the 58th Electronic Components and Technology Conference, Vol. 55, Conf. 2, pp. 1163-1171, 2005.*

[8] *T.C. Chai, et al., "Impact of Packaging Design on Reliability of Large Die Cu/Low-κ (BD) Interconnect," Electronic Components and Technology Conference, pp. 38-45, May 27-30, 2008.*

[9] *F. Sinapi, et al., "Surface Properties Restoration and Passivation of High Porosity Ultra-Low-κ Dielectric After Direct CMP," Micro Elec Engineering, pp. 2620-2623, 2007.*

[10] *J. Bao, et al., "Oxygen Plasma Damage to Blanket and Patterned Ultra-Low-κ Surface," J. Vac. Sci. Technol. A28, p. 207, 2010.*

[11] *L.J. Friedrich, et al., "A Simulation Study of Copper Reflow Characteristics in Vias," IEEE Trans. Sem. Manuf. 12 (3), 353, 1999.*

[12] *L.J. Friedrich, et al., "Study of the Copper Reflow Process Using the GROFILMS Simulator," J. Vac. Sci. Technol. B 15 (5) 1780, 1997.*

[13] *W.W. Mullins, "Flattening of a Nearly Plane Solid Surface Due to Capillarity," J. Appl. Phys. (30) 1, 1959.*

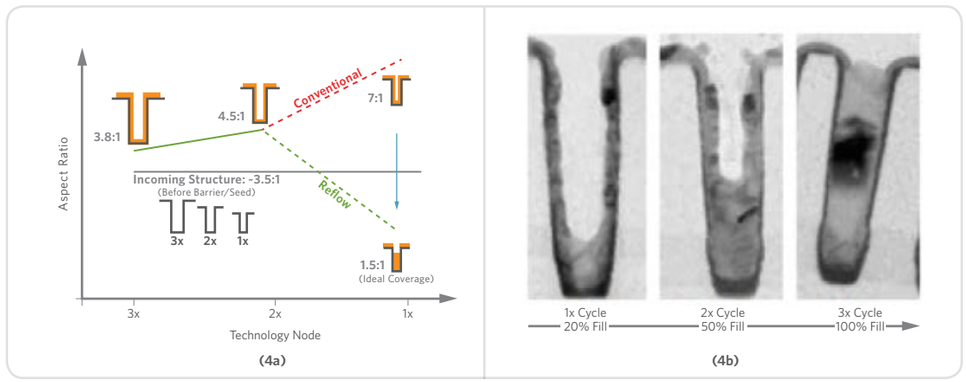


Figure 4. (a) Aspect ratio of interconnect trench after Cu barrier/seed layers and the benefit of reflow at the 1xnm mode. (b) Reflow performance on 2xnm structures.

Thanks to the following individuals for their contributions to this article:

Tom Parrill is director of high-current implant marketing in the Varian Semiconductor Equipment business unit of the Silicon Systems Group at Applied Materials. He holds his Ph.D. in materials science and engineering from Northwestern University.

Tushar Mandrekar is a global product manager in the Silicon Systems Group at Applied Materials. He holds masters degrees in physics and materials science from the University of Illinois at Urbana-Champaign.

Atif Noori is a global product manager in the ALD division at Applied Materials. He holds his Ph.D. in materials science and engineering from UCLA.

Arvind Sankaran is a senior global product manager in the Etch business unit of the Silicon Systems Group at Applied Materials. He holds his Ph.D. in chemical engineering from the University of Illinois at Urbana-Champaign.

Harry Whitesell is a global product manager in the Dielectric Systems and Modules business unit at Applied Materials. He holds his Ph.D. in materials engineering from Auburn University.

Sree Kesapragada is a global product manager in the Metal Deposition Products business unit of the Silicon Systems Group at Applied Materials. He holds his Ph.D. in materials science and engineering from Rensselaer Polytechnic Institute.

For additional information, contact patti_e_seto@amat.com

A REWARDING YEAR

Customer satisfaction is a key measure of business success. In 2012, Applied Materials earned more than 70 awards or commendations from customers in the semiconductor, solar and display industries for support of production ramps, productivity improvement and increased tool and factory output. We are deeply honored.

These customers included:

- AU Optronics Corporation
- GCL Solar Energy, Inc.
- Green Energy Technology, Inc.
- Hua Hong NEC Electronics Company
- Intel Corporation
- JinkoSolar
- Lightway Solar
- Micron Technology, Inc.
- Powerchip Technology Corporation
- ReneSola, Ltd.
- Rexchip Electronics Corporation
- Samsung Electronics Corporation, Ltd.
- Semiconductor Manufacturing International Corporation (SMIC)
- SK Hynix Inc.
- SunPower Corporation
- Taiwan Semiconductor Manufacturing Company, Ltd. (TSMC)
- Tianma Micro-Electronics Co., Ltd.
- Trina Solar, Ltd.
- United Microelectronics Corporation (UMC)
- Winbond Electronics Corporation

MITIGATING THE PAIN OF PARTS OBSOLESCENCE

BY
ADAM KEMPF
AND
AJITH KOTA

Whether your equipment is a legacy 150mm or 200mm workhorse, or a newer 300mm model, it's certainly easy to understand the need for parts re-engineering to keep equipment up and running and as productive as possible. Older parts are often obsolete and simply unavailable, or sometimes the technology changes or just gets better.

The DNA of the industrial supply chain is rife with variables beyond anyone's control. As we pushed Moore's Law from the micrometer into the nanometer over the last 25 years, the required technology and componentry evolved rapidly. Common parts and suppliers were used when possible, but overlap from tool to tool and from node to node often has been limited. The result? With more than 30,000 machines out there, ranging in age from >25 years to hot off the manufacturing floor, Applied has released hundreds of thousands of unique part numbers.

This naturally brings up the question of part obsolescence. There are three main reasons for it, the most common one being low demand. If it's a part that rarely breaks over time, there's little incentive for the part-manufacturer, our supplier, to keep it in inventory. This holds true for our suppliers' supply chains as well. A good example is a CMP polishing platen sub-assembly. One of the sub-suppliers that produced an adhesive in the assembly exited the business because volumes were too low to justify ongoing production, forcing our primary supplier to purchase a new type of adhesive to laminate in house. The new configuration required a new part number and a requalification.

Sometimes, though, an entire assembly may be rendered obsolete because one of its components has become outdated. For example, the processor on a PC board may become obsolete, rendering the entire board useless. A third major reason for part obsolescence is related to performance issues, when a part is subsequently replaced by an updated version. An example would be a vacuum pump with reliability issues relative to newer designs, which is subsequently obsoleted by the pump manufacturer and replaced by a more reliable, improved version.

Obsolescence, in general, is increasingly painful. Applied alone has about twelve thousand 200mm tools installed and currently running in fabs around the world, and they have been processing wafers for decades. The life spans of the tools usually exceeds the life spans of some of the parts inside them. And it's getting harder all the time to find the parts, especially with acceptable quality and at an affordable price. While the incidence rate of obsolescence is higher in older tools, newer tools are not immune, as in the case of the CMP sub-assembly described earlier. As an equipment supplier, we hear you loud and clear on the pain of obsolescence.

CHANGE-MANAGEMENT SUPPORT

We realize that unexpected supply disruptions can wreak havoc with your operations, and that there is no such thing as too much notification. Applied offers comprehensive programs to help mitigate supply chain risk. These change-management programs include supplier risk management and disaster business continuity (most recently tested after the 2011 earthquake in Japan). But at the end of the day, undiscoverable financial, natural or technological disruptions persist.

As a manufacturer, Applied has obsoleted many parts for various reasons. One example was 200mm etch polyimide ESC. Our supplier's particular formulation of polyimide raw material was at risk for obsolescence and we needed to go to another supplier to manufacture the ESC. In this case, Applied re-engineered the material from polyimide to an enhanced polymer. The enhanced polymer ESC (EP ESC) required a requalification in the installed base.

Another example is a CMP membrane. Applied had been purchasing membranes from one supplier, but those membranes were not performing to spec and were sticking to the wafer. In response, Applied qualified a new supplier and obsoleted the original membrane.

Only a fraction of the parts we've obsoleted actually have caused much disruption, but we recognize that obsolescence can be disruptive to a supply chain. Applied is continually working on solutions that will be less disruptive to customers, such as part re-engineering to minimize the impact on your fab operations.

At Applied, we break our parts portfolio into two general categories (see figure 1). Our goal is to better predict the need for replacements of active parts, aligned with customer forecasts. Keeping inventories at the ready for frequently used parts is common practice. Our supply chain network and on-site, near-site, and global inventories are designed to support this goal.

ACTIVE PARTS	IDLE PARTS
• Global usage >1 in last year	• No global usage in last year
• Existing customer forecast	• No forecast
• Targeted stocking level	• No targeted stocking level
	• No recent Applied Materials orders
• ~90,000 parts	**• ~200,000 parts**

Figure 1. Dividing parts into active and idle categories helps Applied align parts-related activities with likely customer needs.

However, it is impractical and unaffordable for any company to stock every part in unlimited quantities. Therefore, we are revamping our active part obsolescence notification processes to reduce the likelihood of unexpected supply disruptions. Customers with Applied Performance Service agreements or specialized parts contracts (for example, Total Parts Management, Applied Parts-on-Demand, or Applied Forecast Order) will receive closed-loop monthly notifications of planned obsolescence for parts, with a goal of providing up to 180 days advance notice. When inventories are sufficient, last-time buys can be processed to postpone the impact on customer operations in line with their product lifecycles.

We're also taking actions on inactive parts to improve the reliability of the information customers receive when ordering less frequently used or "idle" parts (see figure 1). In the past, we quoted lead times and the prices on record from the last order. However, because this subset of parts is prone to the greatest variation in lead times, costs and availability (obsolescence), we have adjusted our order management process for inactive parts to improve accuracy on commitments.

Under this new system, Applied's order-management team will inform customers of the inactive status of the requested parts and verify pricing and lead times before processing orders. Status updates will be provided within the first three business days from order entry, and every 48 hours thereafter until accurate shipment, cost and availability information is locked. If obsolescence issues are identified, customers will be advised and connected to Applied's parts engineering team to determine a resolution with the least impact on customer operations.

We recognize the pain of obsolescence. We understand the pain points and we're taking actions to make it better. We are also looking ahead to further changes that will help you mitigate obsolescence issues on your fab operations.

For additional information, contact adam_kempf@amat.com

BUYING TOOLS ON THE SECONDARY MARKET?

SIX THINGS TO REMEMBER

It's a nightmare: you buy a refurbished tool from a third party instead of the OEM based on a lower price and fast lead time. But the tool is shipped a month late and when it's finally installed there are problems. Parts are ordered and replaced and finally the tool seems ready to run. Then you discover particle contamination from an inadequate refurbishment process. Several iterations and many months later, after spending much more than the price quoted by the OEM, you deem the tool unrecoverable and scrap it. Months of productivity are lost and now you need to buy another tool.

The secondary market for semiconductor production equipment remains strong, driven by devices that don't necessarily require the latest generation of production tools, such as analog and power ICs, microcontrollers, MEMS, and LEDs.

The attractive price of these refurbished ≤200mm tools is often a primary motivation for buying them, but as highlighted in the story above—which is based on an actual experience—buying from a 3rd party, based on price alone, is not without risk.

Here are six "buyer awareness" issues which, in our experience, customers should keep in mind when buying a used tool.

BY T.T. ROBERTSON

1. Predictable Operation

The tool provider and buyer should agree on operational requirements, including an assurance that performance specifications will be met at no extra charge to the buyer. Also, the buyer deserves a commitment as to what date the tool will become operational in the fab.

Buying from an OEM assures that the OEM is knowledgeable about a tool's standard configuration. A third-party provider is unlikely to have this capability. The OEM can also quickly identify any special modifications made by the previous tool owner—modifications that the new owner may or may not want or need. Lacking this information can lead to unexpected and expensive surprises once the tool is installed in the fab.

A third-party vendor does not necessarily provide a warranty. The OEM, however, typically provides equipment support capabilities similar to those it offers on the rest of its tools, covering tool acceptance, process qualification and operation in the fab. For example, Applied Materials' standard warranty on used tools is three months, including corrective maintenance parts and labor, during normal business hours, excluding Applied Materials holidays. Extended warranty and service agreements covering support for multiple years are also available options.

When buying from an OEM, the customer also can be certain that any safety upgrades that were released since the tool went into operation have been included. When buying from a third party, this is an unknown.

2. Ability to Escalate and Fix Problems

The global nature of today's industry mandates an equally global support infrastructure, with material and parts banks and field service operations in close proximity to the equipment. Field service support must be available to fix problems fast, including a well-defined process to escalate to higher levels of the service hierarchy if needed. Equipment issues must be resolved cost-effectively, making it essential that buyers negotiate support guidelines both before and after the sale.

3. Parts Quality Assurance

Tool support includes enabling the buyer to purchase quality replacement parts and consumables from a single, trusted source. The OEM is the one-stop resource to address the full range of part requirements.

Buyers must also beware of used equipment purchased on the open market that may contain damaged or re-engineered parts that do not meet the standards set by the OEM. In fact, often customers buy a tool that looks fine, but they may not be able to identify who manufactured the parts inside. The risk is that an inferior part may not be suitable for the new owner's needs.

For example, implanters include tungsten parts that should be made of 99.9% pure tungsten in order to achieve the tool's maximum allowable metals specifications. But some low-cost brokers supply aftermarket parts made of 80% tungsten, which may work for some applications but can introduce metal contamination issues for other processes.

There are similar issues regarding the implanter's mean time between failures (MTBF) if the vendor does not use the proper parts. That raises the question of how well the implanter will perform over time if the third-party vendor has used low-quality parts in order to sell the used tool cheaply.

4. Obsolescence Concerns

Buyers who try to save by purchasing the lowest-cost tools on the open market can find that needed parts have been made obsolete by the original manufacturer. In other cases, the company that fabricates the parts may have gone out of business.

Purchasing used equipment directly from the OEM can help mitigate obsolescence issues. In many cases the OEM receives notification from suppliers on discontinued parts, allowing the OEM to consider last-time buys to support their installed base. The OEM's engineers can design-in replacement parts that meet all required fit-and-function specifications and are only available from the OEM. Also, OEMs have the specialized knowledge to be able to locate and work with localized suppliers to provide hard-to-find parts.

5. Software Support and Licenses

Given today's highly networked, data-driven fabs, it is vital the tool be equipped with current software. The buyer should be free from worries about whether the desired tool configuration will be achieved, whether they can get newer software revisions if needed, and whether all required software licenses are included.

If a customer buys a tool from another semiconductor company or a third party vendor, the original sale contract regarding the tool will likely specify that only hardware is included, excluding transferability. As such, a buyer needs to make sure they are getting what they paid for: equipment and the software to run the equipment.

6. Known Total Costs—No Surprises

Even when the cost of a refurbished tool takes into account the considerations listed above, there are still opportunities for unwelcome surprises. For example, buyers should be careful to ensure that tools purchased from a broker are not subject to software license fees that were not included in the broker's sale price.

Purchasing refurbished equipment from the OEM provides the buyer with factory- and field acceptance testing, as well as a tool warranty and assurances that current safety standards are met.

A final, very important consideration should be the ongoing investments in development of 200mm technology by the tool supplier. Applied, for example, is one of few OEMs which continue to invest in developing new applications, and in migrating 300mm advances in technology, reliability and cost to 200mm to increase the efficiency and the extendibility of those assets. Many third-party vendors are simply not in a position to afford this continued investment.

The key takeaway for buyers of refurbished tools is that the OEM's name is on the tool, which means that an OEM has more to lose if a customer isn't satisfied. It's the OEM's reputation on the line, and they need to stand by that tool for years to come.

How the used tool performs can impact the potential for the next equipment purchase, whether it is a new or used tool. If it's an Applied Materials product, we want the customer to feel that Applied Materials "did right by me."

For additional information, contact john_c_cummings@amat.com or TT_Robertson@amat.com (implanters)

KNOWLEDGE MANAGEMENT PORTAL

BOOSTS APPLIED'S FIELD SERVICE RESPONSIVENESS

When it comes to installing, repairing, maintaining and upgrading highly complex production tools for semiconductor, solar and display applications, the proverb "time is money" couldn't be more apt.

The longer a tool is down, the more revenue a fab stands to lose. Today's faster paced and fickle markets mean the economic impact of idle equipment may be greater than ever. Whether manufacturers perform service in house or use an outside service provider, the need is always the same: a fast, expert response to get tools up and running as quickly as possible.

Maximum service responsiveness and speed come not only from product experience and technical training, but also from the engineer's ability to quickly leverage company resources. These resources include product documentation, best known methods (BKMs), product notices, parts information, service bulletins and manuals, bills of materials (BOMs) for specific tools, images and other information that may be needed to perform the service.

The faster company resources can be accessed, the faster customer problems can be resolved and BKMs implemented to reduce downtime. To accomplish this, Applied has implemented a customized, searchable and secure internal knowledge management portal for its service engineers known as Applied Rapid Knowledge (ARK).

ARK is an innovative and comprehensive search engine that enables engineers to find documentation and other information from multiple data sources using a single, simple interface. ARK includes collaborative features that let users provide feedback on product manuals, customer engineering notices, internal service bulletins and parts. The portal also allows users to share BKMs across the organization.

More than 12,000 service-related documents, 2 million part numbers, and all tool "as shipped" BOMs can be searched in ARK. Hundreds of new and revised documents are added monthly. They are organized and updated by a content management system that employs standard practices and taxonomy to assign key attributes and terms to documents to facilitate searches. This allows new documents to be searchable immediately.

Through ARK, information that was previously difficult to find or that may have been distributed across a number of sources is more easily accessible. Since ARK went online in May 2012, Applied's field service engineers have reported an average 50% reduction in time spent searching for information, with a roughly 10% improvement in document accuracy, based on before and after tests. This reduction has significantly improved the engineers' efficiency. On average more than 90 unique users access the ARK portal each day and that number is trending upward.

"The ultimate value our service business brings to our customers is our ability to help them earn revenue by reducing or eliminating equipment downtime," said Cassio Conceicao, vice president of Applied's service products group. "ARK helps us do that better and faster, by putting necessary information at the fingertips of our expert engineers with precision and speed."

For its achievement in developing and implementing the ARK portal, Applied Materials was named to the 2012 InformationWeek 500 list of business technology innovators.

REPORTER'S NOTEBOOK:

DAVID LAMMERS

A VIEW FROM BELGIUM

As many big corporate research labs, from Bell Labs to Hitachi's Central Research Laboratory, have been scaled back, consortia such as imec, in Leuven, Belgium, are performing more of the basic semiconductor research. But while much of the "R"—research—of the semiconductor process R&D budget is outsourced to consortia, the "D"—development—is closely guarded within companies. For the two dozen journalists invited to Leuven in October 2012 for the annual imec Technology Forum (ITF) for media, the event was an important update on the direction of leading-edge research.

People in other industries, such as pharmaceutical, are amazed at how open companies in the semiconductor industry are within these research consortia. One compelling reason is that the challenges are becoming more expensive: IC Insights estimates that R&D spending by semiconductor companies worldwide is expected to grow 10% in 2012 to $53.4 billion, a record high.

Luc Van den hove, chief executive officer, imec-NL

Luc Van den hove, imec's CEO, said the challenges facing the chip industry can seem overwhelming, ranging from EUV lithography, which tops his list, to keeping process complexity and costs under control. However, "we shouldn't overemphasize the difficulties," he said, in part because the work is somewhat divided.

Intel took the lead on FinFET development, while ASML is the center of EUV research. Equipment companies will do most of the 450mm tool R&D.

Imec has a much different role in the 450mm transition than the Global 450mm Consortium (G450C) based in Albany, New York. Albany will focus on developing the automation and process equipment needed to process 450mm wafers, while imec's role is to serve in the development of CMOS process technology on 450mm wafers.

"There is no sense competing with Albany. Our role is to enable scaling," said Van den hove.

"EUV is the most important issue. If we don't get it to work on time, then the cost of scaling will be phenomenal. That would slow down scaling," he said.

Investments in ASML by Intel, Samsung and TSMC will enable "the right critical mass of people" working on EUV lithography. "More money equals more people, resulting in faster solutions," he added.

Van den hove noted that scaling is already slowing down. At the 14nm node, companies are likely to introduce a first version, based on FinFET devices, using double patterning with 193nm scanners. This first-generation 14nm node would not have the SRAM density doubling seen normally from node to node. When EUV becomes fully available, a second 14nm technology would be introduced with smaller transistors. And because EUV involves fewer masks than double patterning, the costs of this second generation may improve as well.

Other technologies will support the chip industry's progress, including optical chip-to-board interconnects, through-silicon vias, vertical NAND, and larger 450mm wafers. Already, imec researchers are seeing sharp reductions in gate leakage by adding aluminum to today's hafnium oxide high-k dielectrics. And several CVD-type low-k dielectrics will reduce R-C delays in the interconnect stack. Directed self-assembly (DSA) copolymers are now beginning the arduous journey from lab to fab, and may ease the burden on EUV lithography.

An Steegen, senior vice president of process technology, imec-NL

An Steegen, a former IBM researcher who now heads up imec's CMOS scaling efforts as senior vice president of process technology, envisions another major change at the 10nm node. By then, leading-edge devices will require high-mobility channel materials, including germanium in the P-channel and III-V compounds such as indium gallium arsenide in the N-channel.

"We have to solve the epitaxial challenges," Steegen says, referring to the lattice mismatch issues that challenge the introduction of III–V materials.

All these technical challenges, which may seem overwhelming when taken together, seem to bring a kind of determined good cheer to the imec researchers. The industry's myriad R&D projects are "job security for us," said Van den hove. "Things are not at all easy right now. While the challenges are unprecedented, the main players are also getting bigger."

Imec is located in Flanders, the Dutch-speaking portion of Belgium, which funds a small fraction of imec's €300 million budget.

The most tangible return on the Flanders government's investment is the 2,000 people who work at the imec campus, reason enough for Flanders to invest about $130 million (€100 million) towards a billion-dollar 450mm clean room, which is now in the planning stages.

And that leads back to the hope that more R&D money will bring in more people with the skills to solve the semiconductor industry's challenges. Van den hove sees employment at imec going up by 500 people in the next five years.

LAST WORD

David Lammers is an Austin-based technology journalist who has worked at EE Times, Semiconductor International, and Semiconductor Manufacturing and Design.

APPLIED MATERIALS®

www.appliedmaterials.com

Printed on Recycled Paper

AGS-NFS-1212 12/12 5K

Applied Global Services

AMPLIFY your Return™